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DEVELOPMENT OF STANDALONE SOLAR PHOTOVOLTAIC INVERTER WITH HARMONIC ELIMINATION TECHNIQUE

[1]A. Akshara, [2]M. Malukannan, [3]S.krishnan

[1]ME, Control system, Mahindra engineering college Namakal, Tamilnadu India
[2]Assistant Professor, Department of mechatronics
[3]Assistant Professor, Department of EEE

Abstract:*This paper proposes a photovoltaic (PV) array based cascaded H-bridge multilevel inverter (CHBMLI) working active power filter as a shunt for four wire distribution system. This system is used for the power acclimatizing of distribution network as it is composed of linear, nonlinear and unbalanced loads. Solar Photovoltaic formed isolated source for CHBMLI. This active filter minimize line harmonics, minimize neutral wire current about to zero and it also injects real power as per requirement of the system. The grid interface and required reference signal generation is carried out with the help of Instantaneous power theory. The simulation studies are carried out in MATLAB Simulink environment.*

Key Words: Photovoltaic array, Cascaded H-bridge multilevel inverter (CHBMLI), Nonlinear and Unbalanced load, Harmonics compensation, Active and Reactive power.

I. INTRODUCTION

Solar photovoltaic systems are very popular as they are clean, inexhaustible and require little maintenance. With rapid depletion of fossil fuel it is evident that energy requirement has to be supplied from renewable sources and solar generation will be a major contributor. Worldwide 164 countries have adopted at least one type of renewable energy target [1]. EU plans to generate 20% of it requirement from renewable sources by 2020. In January 2015 Govt. of India significantly expanded its solar plans, targeting 100 GW of solar capacity by 2022. It is expected that additional 10,000 MW of solar power plant will be installed by 2017. Conventionally two-stage grid connected solar PV system are used, in which the first stage performs MPPT (maximum power point tracking) and the second stage is used to feed extracted energy into the grid [2-3].

Some researchers have also proposed two stage grid connected solar PV system with additional features such as active filtering, reactive power compensation etc. [4-5].

Recently the single-stage SPV systems are introduced by some researchers. These are small inverter installed in distributed generation system and hence reduces the distribution losses. Single-stage multifunctional grid interfaced solar photo-voltaic system is proposed by [5-9].

However, the inverter used for grid connected solar PV system will inject harmonics in the system and will causing serious power quality problems [10]. With an expected target of 100GW generation from solar PV system grid will be highly polluted with harmonics. This paper, proposes a multi-level inverter topology for grid connected solar inverter which in turn will reduce the harmonic injection in the grid. Paper also proposes an optimal solution for the number of inverter level that will maximize the system efficiency.

II. RELATED WORK

There are a few classics multilevel inverter topologies. These classes are the neutral point clamped topology (NPC) [9–11], the fying capacitor topology (FC) [12, 13], and the cascaded H-bridge topology (CHB) [14–16]. NPC inverters are widely used in photovoltaic systems due to their characteristics of low switch losses, and freedom from common-mode leakage current. However, all of the NPC inverters need to solve the problem of capacitor voltage balance on dc side. CHB inverters can heighten the voltage rank by series connections. However, CHB converters require multiple sets of isolated dc sources, which is a main drawback of this topology.

Topologies with the multilevel structure have good output characteristics due to their ability to produce staircase-like voltage waveforms. However, multilevel inverters exhibit an important limitation. For an increased number of output levels, they require many power switches, which increases the cost, control complexity and the losses of devices [17]. In photovoltaic applications, the output power of PV cells spans a wide range and varies greatly [18–21]. Due to the wide input range of inverters, the power levels of the power devices and flter inductor are selected from the maximum output

power. This leads to high device cost, high losses and low system utilization. There is a contradiction between achieving a wide operational range and reducing power losses [22, 23]. For the past few years, efforts have been directed to reduce the cost and losses in multilevel inverters, and many topologies have appeared.

In [24] and [25], a T-type inverter with a significant reduction in the number of power devices was described. In addition, this topology can be applied to any number of voltage levels within the switch maximum voltage. In [26], a multilevel inverter using the series/parallel conversion of dc voltage sources was proposed. When the capacitors are connected in series, the voltage of devices is reduced, as well as the total losses of the devices. In [27], a flying capacitor clamped inverter based on a switched capacitor was proposed. Its modulation strategy reduced the losses of the switch devices by curtailing the switch frequency of certain switches. In [28], an H-bridge inverter with dc side switches was proposed and applied to a PV system. In this topology, the bridge arm switches operate at a low frequency, which reduces the switch losses. The above inverter topologies reduced losses by optimizing the topology structure.

III. MATERIALS AND METHOD

The proposed work uses 27 level inverter with reduced switch topology to get better reliability with low harmonics. This inverter performance completely relies on EANFIS controller which is the combination of ANFIS and Emperor Penguin Optimization (EPO) algorithm. Working procedure of ANFIS will be optimized by EPO to make us easy to grip transferring position of MLI and make less harmonic controller voltage. Main concept of EPO based on huddling characteristics of emperor penguins. While comparing with other met meta-heuristic algorithms, EPO provides efficient result by means of computational complexity, time and space complexity. This is the main reason to select EPO for optimizing ANFIS controller in our proposed work.

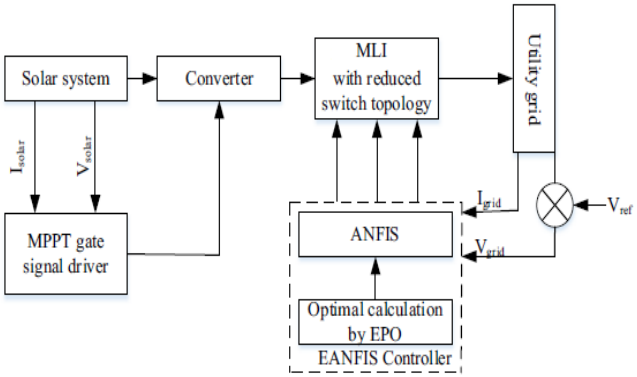

Figure.1. Block Diagram of Proposed System

Diagrammatic flow of proposed work given in Fig. 1. Solar fed to 5 level MLI with minimize switch topology. Data required for EANFIS obtained by solving harmonic equations by considering various modulation indices. THD evaluated from output voltage generation of EANFIS controlled MLI. Main focus of EANFIS controller is to make inverter to harmonic free output voltage similar to grid voltage. Here, no essential of filter circuit to improve inverter output because of generation of harmonic less output at inverter side. Thus proposed EANFIS controller perform better in THD and reduce design complexity of whole system.

3.1 SOLAR PV ARRAY:

The building block of PV arrays is the solar cell, which is basically a p-n semiconductor junction, shown in Fig.2. The V-I characteristic of a solar array is given by Equation.

$$I = I_{sc} - I_o \left\{ \exp\left[\frac{q(V+R_s I)}{nkT_k}\right] - 1 \right\} - \frac{V+R_s I}{Rsh} \quad \ldots (1)$$

Where:

V and I = Output voltage and current of the PV, respectively.

R_s *and* R_{sh} = Series and shunt resistance of the cell.

Q = Electronic charge.

I_{sC} = Light-generated current.

Io = Saturation current

N = Dimensionless factor.

K = Boltzmann constant,

Tk = temperature in o^K

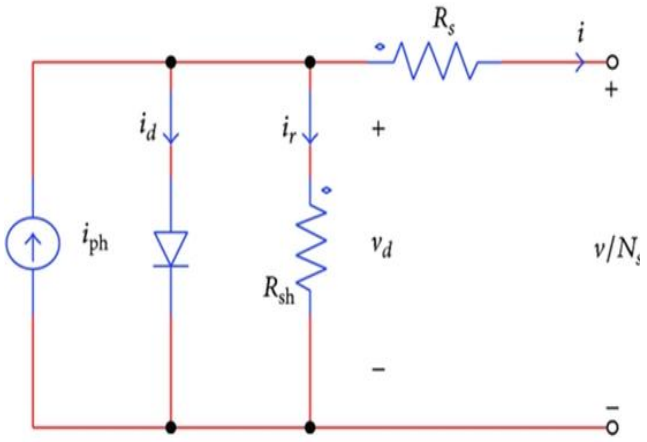

Fig 2: Equivalent Circuit of PV

Equation (1) was used in computer simulations to obtain the output characteristics of a solar cell, as shown in Fig. 2. This curve clearly shows that the output characteristics of a solar cell are non-linear and are crucially influenced by solar radiation, temperature and load condition. Each curve has a MPP, at which the solar array operates most efficiently.

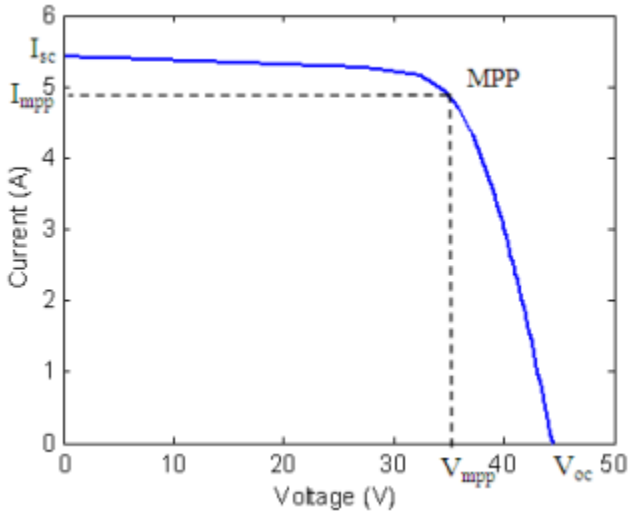

Fig 3: Characteristics of Solar Cell

3.2 ANFIS FOR MAXIMUM POWER POINT TRACKING:

ANFIS was made given a perception out of P-V trademark curve. This method was wanted to solve the few disadvantage of the P&O technique. ANFIS tries to upgrade the following time and to make more power on an enormous light changes condition [4]. The maximum power point (MPP) can be registered by using the association between DI/DV and – I/V. On the distant possibility that DP/DV is negative, by then, MPPT is lying on the right side of the present position, and if the MPP is dynamic, the MPPT is on the left side. The state of IC technique is

$$\frac{DP}{DV} = \frac{D(V.I)}{DV} = I\frac{DV}{DV} + V\frac{DI}{DV} \quad \text{.....2}$$

$$\frac{DP}{DV} = I + V\frac{DI}{DV} \quad \text{.....2}$$

MPP is reached when DP/DV = 0

$$\frac{DI}{DV} = -\frac{I}{V} \quad \text{.....3}$$

$$\frac{DI}{DV} > 0 \; then \; Vp < Vmpp \quad \text{..... 3}$$

$$\frac{DP}{DV} = 0 \; then \; Vp = Vmpp \quad \text{..... 4}$$

$$\frac{DP}{DV} > 0 \; then \; Vp > Vmpp \quad \text{..... 5}$$

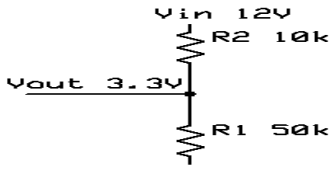

Figure 4. Voltage Divider circuit

$$\text{Vout} = \left(\frac{\text{R2}}{\text{R2+R1}}\right)\text{xVin} \quad \text{.....6}$$

Where Bout=output voltage feed to microcontroller taken as 3.3volt, R2=10k ohm R1= resistance that user has to calculate, Vin= open circuit voltage of SPV panel

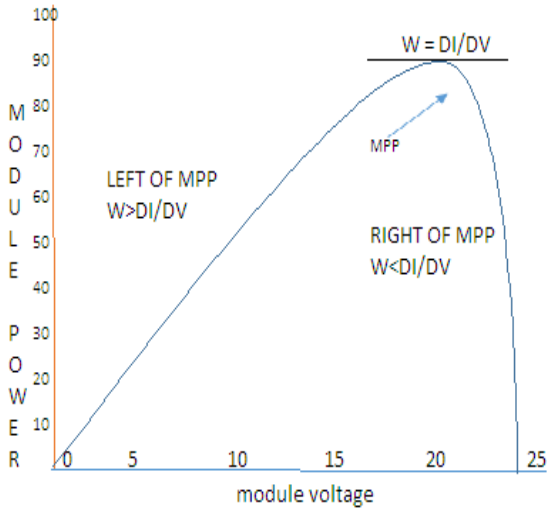

Fig 5: PV – curve model of solar module using ANFIS

The ANFIS relies upon the way that the incline of the PV exhibit power curve is zero at the MPP, dynamic on the left of the MPP, and negative on the right, as given by DP/DP = 0 at MPP

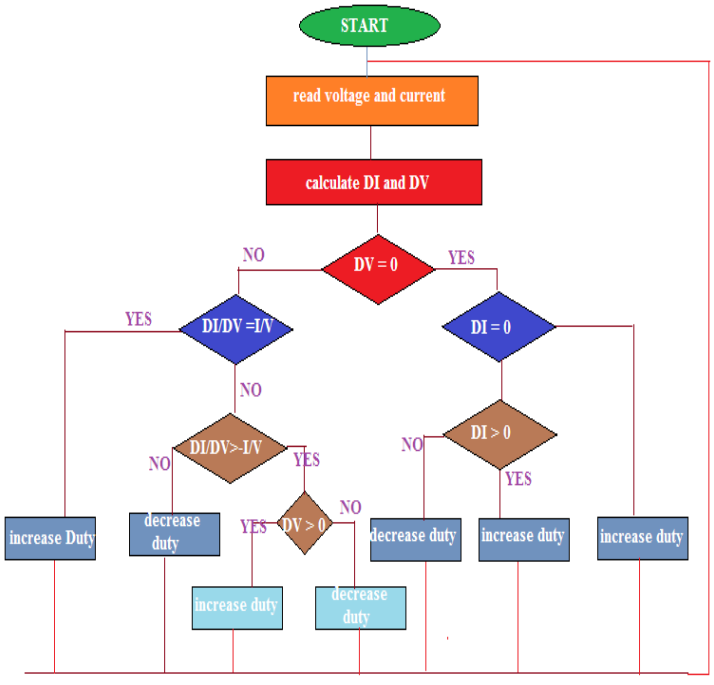

Figure 6. Flowchart of ANFIS – MPPT Method

ANFIS technique can be found in Fig. 6. In case MPP lies on the right side, DI/DV< - I/V and from that point forward, the PV voltage must be decreased to go to the

MPP. The IC system can be used for finding the MPP, upgrade the PV capability, diminish control incident and structure cost. Execution ANFIS on a controller made an all the more consistent execution when it stood out from Perturb and Observe (P&O). The swaying around MPP zone also can be covered in a trade-off with its use multifaceted nature. The accompanying time still not fast since the voltage expansion and decrement had been picked physically by experimentation.

3.3 BOOST CONVERTER:

The converter is related to the DC-bus, and the AC-bus as showed up in Fig.7 mentioned above. Its act as a bidirectional converter based on the inverter workflow, where it fills in as an inverter to switch the power from the PV (or the battery bank) to the AC load, and as a rectifier for a circumstance of charging the battery bank from the solar board. The converter is shown in light of its assessed utmost and profitability, which are believed to be steady every through it working reach.

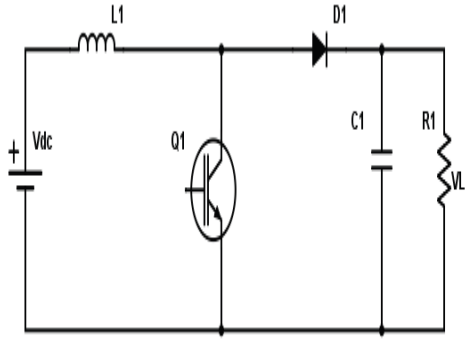

Fig 7: Boost Converter

The general plan conditions of the boost converter are given below

$$VL = \frac{Vs}{1+\sigma} \dots (7)$$

Where VL is the output voltage, vs. is the source voltage, and σ is the duty cycle. In the continuous conduction mode (CCM) the base inductance of the Lmin is expressed as

$$L_{min} = \left((1-\sigma)^2\right)\sigma Rl\right)2f_s \ldots (8)$$

The capacitor esteem is composed to such an extent that the voltage swell Vr as

$$C_{min}\ \sigma/Rlf_sV_r \ldots (9)$$

The output voltage relies on the estimation of the obligation cycle which is in charge of the steady output voltage. The load current Io with the duty cycle is expressed with source current Is.

$$I_o = (1-\sigma)I_s \ldots (10)$$

The variation of the current ∇I based on the inductance was expressed as

$$\nabla I = V_s(V_l - V_s)/f_sLV_l \ldots (11)$$

3.4 INVERTER:

The DC voltage is changed over into AC voltage, and it is sustained to the BLDC motor. The inverter utilized here is voltage source converter with PWM method using VTO. Synchronization must be legitimately done to guarantee the PV panel is nourished appropriately into the BLDC drive. Outline condition inverter is taken after. Base esteem is presented which goes about as reference, and it is given as

$$X_b = (E_n)^2P_n \ldots (12)$$

$$B_b = 1/(W_nZ_b) \ldots (13)$$

$$W_n = W_b \ldots (14)$$

Where

W_n = Grid frequency, E_n = RMS Voltage and P_n = Active power. The DC side Capacitor is selected based on following conditions.

1. Time delay which is introduced by filtering of the DC voltage and Current control Tr.
2. DC voltage variation ΔV_0
3. Maximum power variation ΔP_{max} on the dc bus
4. Load ride through ability and assurance amid utility voltage hang occasions The DC capacitor can be planned to utilize the accompanying condition

$$C \geq \frac{Tr\Delta Plmax}{2V_0\Delta V_0} \ldots (15)$$

An LCL channel arrangement is actualized to take out the switching frequency harmonics given the angle of the voltage and current sensors the capacitor variably affects the framework. The AC side capacitor value is calculated as

$$C_f = l - \frac{lG}{2b^2} \ldots (16)$$

The magnetic core used for the design of inductor is made up of following materials laminated metal alloy, iron, ferrite and powdered metal. The present ripple produced by the VSC is restricted by the inductance L which is on the converter side. The present ripple is expected to the VSC switching. The converter side inductance is given by the underneath condition.

$$l = \max(V(n)/nW_b I_{Limit}(n)) \ldots (17)$$

Where v (n) – voltage generated at n-harmonic by the VSC and $I_{Limit}(n)$ is the maximum passable current ripple at the n-frequency. The satisfactory switching ripple is utilized to decide the inductance lg at the inverter side.

IV. RESULTS AND DISCUSSION

The proposed work will be implemented in Simulink working environment. Resultant outcomes like inverter output, controller output and THD analysis will be compared with recently developed existing works. Our proposed work is compared with existing PID and PI controllers. Figure 8displays the proposed model of Simulink.

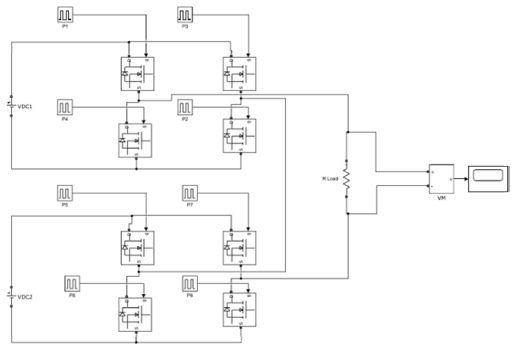

Figure 8. Simulink Model

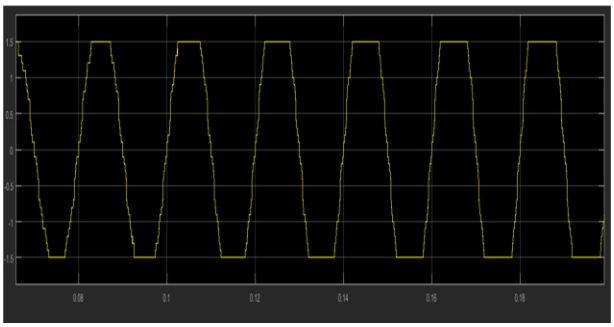

Figure 9. Inverter Current

Figure 9displays the performance of inverter current. By varying EANFIS controller, the inverter current performance are taken. By using this controller for tuning the purpose of the inverter we got stable inverter current.

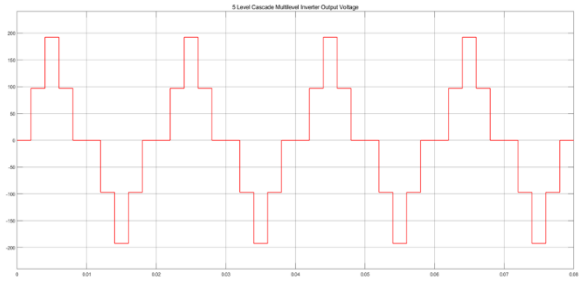

Figure 10. Inverter Voltage

Figure 10 gives the performance of inverter voltage. By varying EANFIS controller, the inverter voltage performance are taken. By using this controller for tuning the purpose of the inverter we got exact inverter voltage. Our proposed method give better result give better results compared with others.

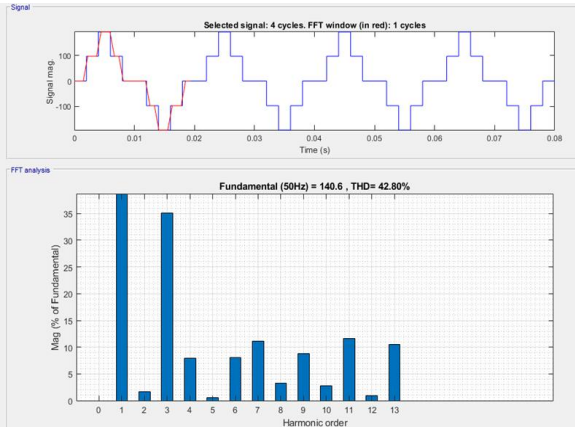

Figure 11. Simulation Result of THD

Figure 11 shows the performance of THD waveform for the yield voltage at the load side. In the proposed system the THD value in load side is 0.78%.

V. CONCLUSION

In this paper solar fed to 5 level MLI with minimize switch topology. Data required for EANFIS obtained by solving harmonic equations by considering various modulation indices. THD evaluated from output voltage generation of EANFIS controlled MLI. Main focus of EANFIS controller is to make inverter to harmonic free output voltage similar to grid voltage. The proposed work has implemented in Simulink platform. The expected outcomes like inverter current and voltage, grid current and voltage and THD analysis will be compared with recently developed existing works. Our work is compared with existing PID and PI controller. In future, the level of multilevel inverter is analysed in real time environments with the help of experimental setups.

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