Scientific Journal Impact Factor (SJIF) : 5.278
International Journal of Modern Trends in Engineering and Research
ISSN (ONLINE) : 2349 - 9745
ISSN (PRINT) : 2393 - 8161

DESIGN AND ANALYSIS OF CMOS LOW NOISE AMPLIFIER BASED FOLDED MICRO STRIP PATCH ANTENNA FOR WIDEBAND APPLICATIONS

[1]N.Vidhya PG scholar, [2]B.Prasad Ph.D

[1,2]Department of ECE, Dhirajlal Gandhi College of Technology,Salem, Tamilnadu, India.

ABSTRACT: In this work, co-design of LNA and Folded micro strip patch Antenna is addressed over wide band frequency 10-20 GHz. The main motive of co-design is to relax the impedance matching on LNA as well as Antenna. Antenna designed is Micro-strip patch antenna provided with micro strip feed at the ground plane for maximum signal receiving and T-slot is provided at the center of the patch so that it provides wide range of frequency for excitement of electrons. The co-designed LNA benefits from a size, cost and noise figure reduction. The antenna input impedance has no more to fit constant and real impedance on the whole bandwidth. In the present case, this point is used to reduce dimensions. Measured results agree well with the simulated ones, giving a wide impedance bandwidth from 1.68 to 2.75 GHz, a high port-to-port isolation (better than 37 dB) within the operating frequency bandwidth, and a good radiation pattern.

Key words: Polarization Conversion Meta- material, Advanced Design System, Low Noise Amplifier, High frequency Structural Simulator, Radar Cross Section

I. INTRODUCTION

Satellite telecommunications has played a major role not only for communications but for military purposes also. It provides more information as it provides broadband and Internet service continuous future generation networks should play an important role. Satellite receiver systems require a low noise amplification, which is much smaller and has been placed right of the antenna to increase signals. The transmitting signals have been one of the key factor in the receiver's quality factor, due to the absence of the noise rate from the first amplifier to the amplitude of the receiver. The purpose of this work has design a wideband LNA with a low noise figure to get as possible high. Two-stage LNA design to gain the advantage of the need for a system with no noise bandwidth. The first level will be to optimize noise of figure, bandwidth and overall gain is increased in the second stage. The most surface of the Earth's surface is highly detailed by North Atlantic Space Administration (NASA).Because the radio frequency zone gets reflected by it. In a global positioning system, high permittivity molecular material used in the Micro patch antenna containing the base of Low noise amplifier (LNA) and the Basic Structure of Micro Strip Antenna is shown in Figure.1.

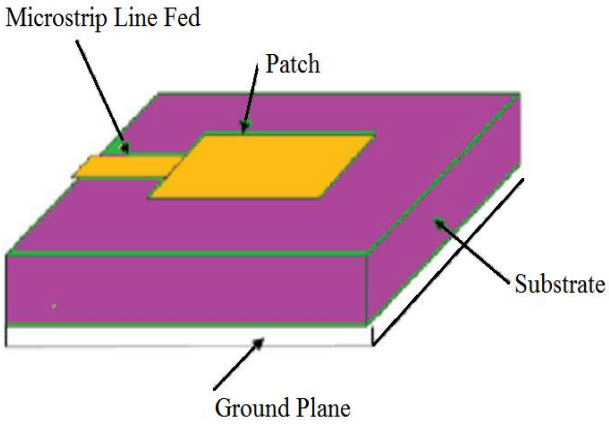

Figure.1.Basic Structure of Micro Strip Antenna

The Low noise amplifier (LNA) has been one of the main component of the wireless transceiver circuit and its play a very significant role in determining the receiver's capacity. Wideband LNA is based on a wavelength based on more than one or more of the same operating characteristics over wideband applications.

II. LITERATURE SURVEY

Over the past few years, redesigned antennas have become the attraction-design approach to the standard antenna replacement which offers properties that emit vibration and bandwidth for various wireless applications like it. The frequency band feature is usually derived from a Varactor diode or a reversible combination of denial which is provided by the rectifier and RF diode [1-5]. Frequency redesigned antennas are capable of altering the frequency of their vibrations has to beoperate on particular bands along with several servo spectrum radio system [6-7]. Critical advances on frequency dynamic antennas have been accounted for over the most recent couple of decades, for example, in [8-10]. A patch antenna radiating edges has been with electronic tuning frequency reconfigurability, while a PIN diode switch controls the current path length of the connector surface, to allow Varactor diodes to be loaded [11-12]. In [13], Micro strip Transmission Line model was calculated from the antenna designs, which is known as any popular model. A quick and easy model when a mathematics is set up with a software package and the TLM is given as a symmetrical feed

Complementary Metal Oxide Semiconductor (CMOS) innovation is as yet considered a fitting decision because of its various focal points, for example, cost, little size, low power utilization and abnormal state of reconciliation. Despite the many advantages, the CMOS for receiver applications faces difficulties to have multiple challenges and [14-15] in the Low Noise Amplifier (LNA) design. Technologies for the CMOS based on LNA have been announced by a number of previous researchers.

@IJMTER-2020, All rights Reserved

III. PROPOSED METHODOLOGY OF OPTIMIZED LNA DESIGN

The LNA essentially consists of three sections that are designed to be round the whole network, which correspond to output matching network, main transistor section and input matching network. In Low noise amplifier designing, following important goals are achieving get the higher gain, minimum power consumption, low Figure of Noise and get perfect input/output matching. The transistor should be dependent on the appropriate operating system before using. So, it can work under required values and achieve lower power consumption. The proposed Patch Antenna Block Diagram is shown in Figure.2

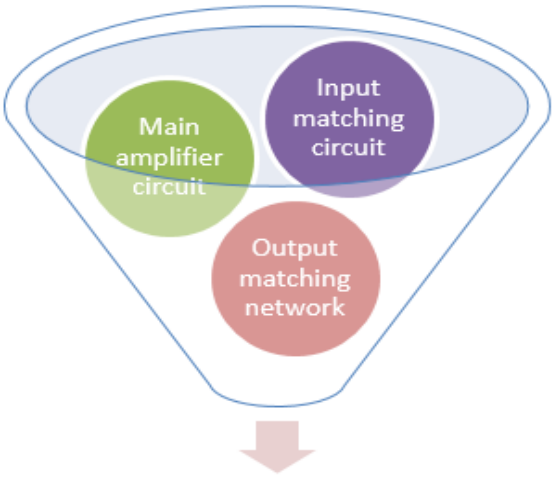

Figure.2 Block Diagram of proposed Patch Antenna

Input the shared network should reduce the input back loss without starting additional noise. Since the noise point of view, we need a change network so that LNA can be the first to get the minimum NF. LNA 50Ω block impedance capabilities have been created. The amplifier provides the highest gain, high linear low noise factor and low power consumption and at the same time it provides input impedance that can be adapted for wideband matching.

The network of output matching circuit comprise of capacitors (C5 &C6) and inductor L6. Here the capacitor C5 is serially connect with Parallel combination of C6 and L6. The output is designed to get a better fit between LNA and mix input like this. It also prohibits noise as much as possible to provide good fit between LNA and mix input.

3.1 PROPOSED LNA WITH GAIN OPTIMIZED

The LNA needs to be recycled in a low cost efficient and optimized manner, the target wave band (5.4GHZ) provides low noise, high stability and high gain. The LNA is built using a network that matches the general common source (CS) input that applies to the terminal in its matching network of its drain terminal of M1, the output applies. Figure.5 showsthe

proposedarchitecture of the newantennatopology.The gain mode pair first improved gain that connects the parasitic Capacitor C3 and C4 to each other's source of M1 and M2. The M2 and M1 has twice as much as any extra DC power consumption with the opposite signal combined with each other's capacitive-cross combinations due to the successful transmission of input signal. When connecting L3 and L4 as the M2 and M1 source, this circuit is configured in an advanced gain mode under the general gateway connection antenna using the high-order LC arrangement.The Connection Antenna then has a single completed input differential output LNA system.L3and L4 cannot find the board in order to present full configurability, or if the target input version is fixed they require higher synchronization status where the on-chip can be placed.At the time left to connect to an M2 source as only an anchor and the M1 source on the L4 to ground, WhereM1 is act as gate input stage and M2 act as a common source input stage, respectively

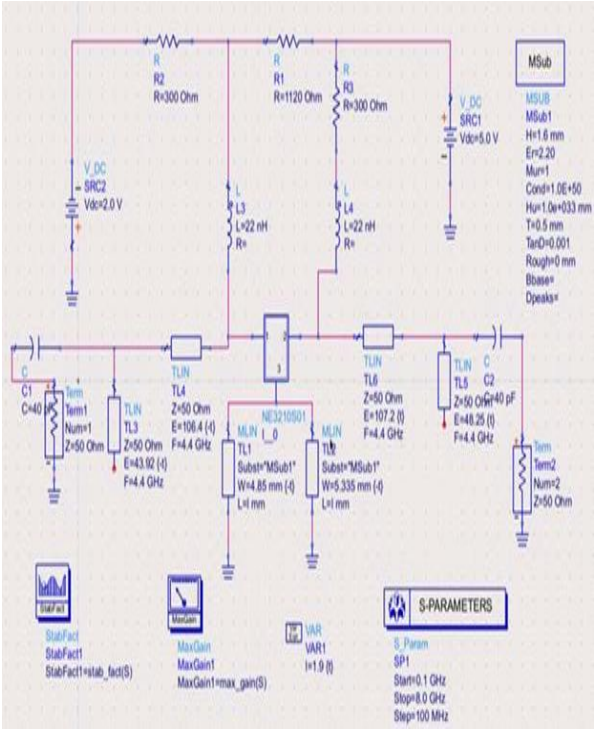

Figure.3.Proposed Low Noise Amplifier (LNA)

As shown in the Figure 3, the electric inductor L3 and L4, together with the resistor R1 and R2, mount the antenna working frequency band to improve the low quality factor set the 2nd Order Resonance Load. Together with the cascade pair M3, M4 and C2 of the cascaded pair M1, the Inter Stage Resonance L3 and L4 with the parasitic capacitor C1. This inter-platform technique has been used in the previous ultra-bandwidth attachment antenna design, but the main purpose is to remove the cascade of noise level in high frequency.The impact of the connection bandwidth is not fully emphasized.

@IJMTER-2020, All rights Reserved

3.1.1 Gain optimized recycle mode

In order to achieve low power consumption and high profitability, the system is improved in recycling system. Optimized recycle mode system layout design is easy to setup. In order to gain a simplicity power, the network is designed to compensate for the benefit of the network. LNA design is also used in improved recycling architecture shown in Figure 4.

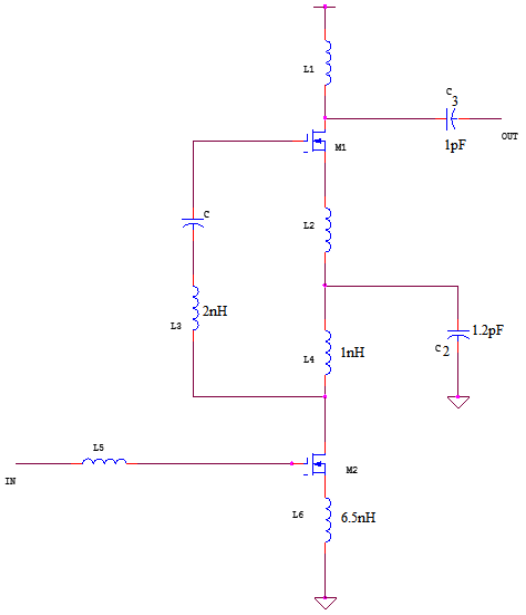

Figure.4. Recycle mode Structure of Gain Optimization

Recycle mode Structure of Gain Optimization circuit comprise of Inductors (L3 & L4), capacitors (C2 & C3) and MOSFET (M1). In this circuit inductor L3 is directly connected to gate pin of MOSFET , inductor L4 is connected to source pin of MOSFET with shun arrangement capacitor C2. Here shunt capacitor C2 has been utilized to resonate the parasitic capacitance of M1. Meanwhile high impedance path has generated using L4 and a sourcedegenerated inductor L6 has been connected to increase the gain ratio.

IV. SIMULATION RESULTS

Advanced Design System software is used to design and measure the parameters of LNA with 0.18µm CMOS technology. Various simulation parameters will be discussed in the following figures, the wave ratios, wave ratio, gain, input reflection coefficient, output reflection coefficient, reverse isolation factor, stability factor, noise count, supply voltage, including wave proportion, range voltage (M1 / M2) Power consumption and gate source voltage.

The Figure of Noise ratio analysis of proposed antenna design is shown in Figure.8. Based on the response of desired frequency the proposed LNA receives a best result of noise ratio for 0.423.

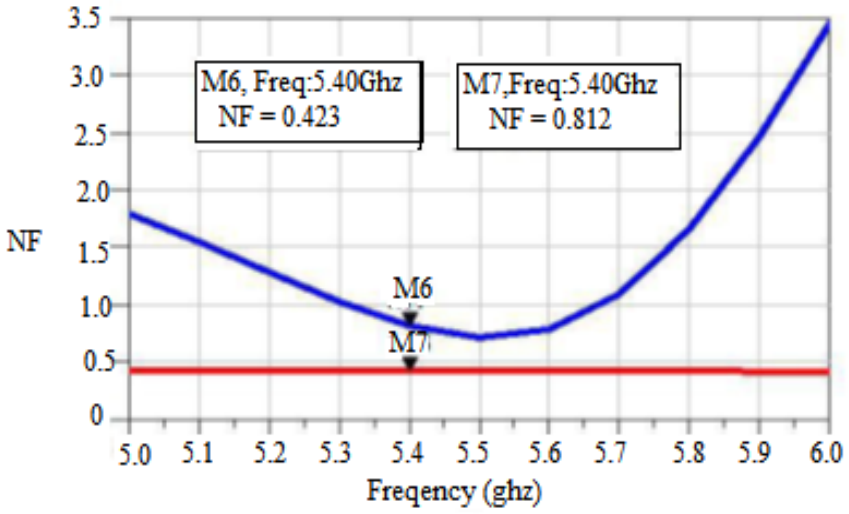

Figure.5. Noise Figure

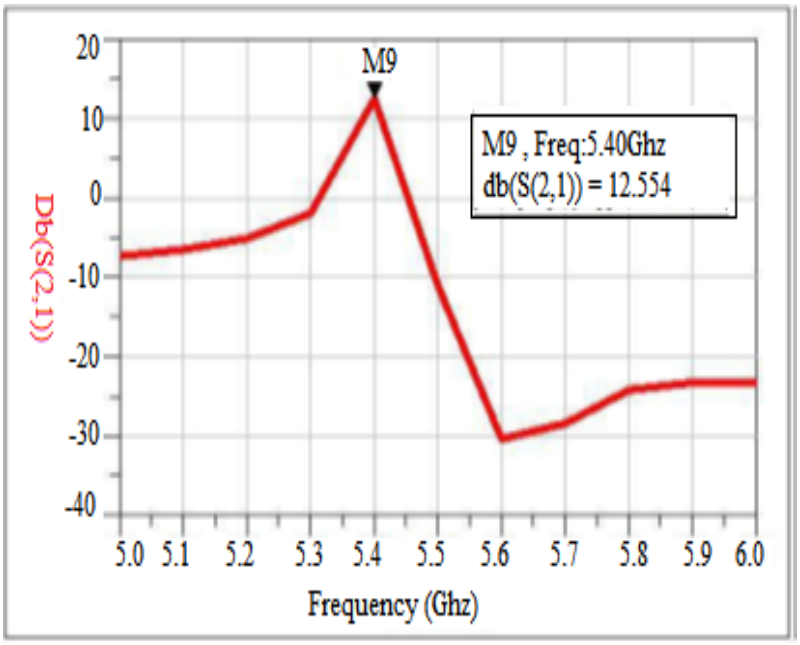

Figure.6. Gain Analysis

The gain analysis of proposed antenna design is shown in Figure.8. Based on the response of desired frequency the proposed LNA receives a maximum gain value of 12.554dB

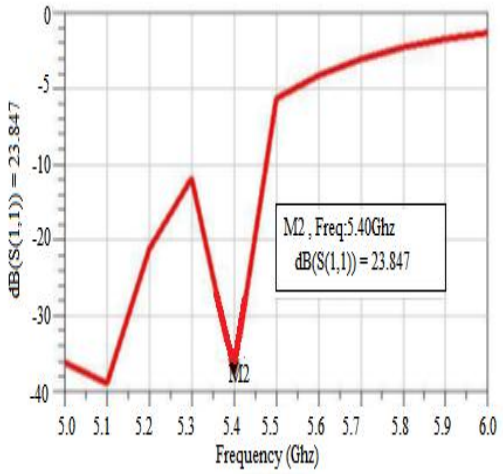

Figure.7. Input Side Reflection coefficient analysis

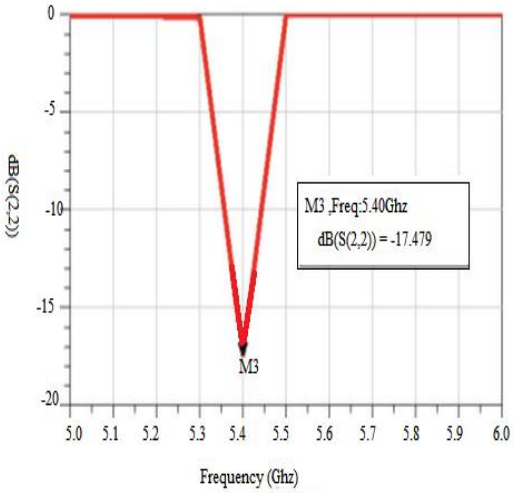

Figure.8. Output Side Reflection coefficient analysis

The input and output side reflection coefficient analysis was demonstrated in figure 1 and 10. The proposed matching circuit give the best matching response, for example the input value of reflection coefficient is -23.846db at the same time output side reflection coefficient is -17.486db.

Table.1. Performance Comparison Proposed LNA

Comparison between the proposed work and various components of various LNA designs in the creation works is Table 1, which is summarized in a table below. This table enables us to provide an effective low amplification amplifier.

Parameter	4	3	6	7	8	12	19	Optimized recycle mode
CMOS Technology(μm)	0.18	0.18	0.18	0.18	0.18	0.18	0.13	0.18
Frequency (GHZ)	5.8	3-16	5	5.4	5.4	5.2	3.1-4.8	5.4
Noise Figure(dB)	0.97	4.2	1.9	2.4	<3	2.94	3.5	0.423
Power dc(mW)	6.4	11	12	1.6	2.7	4.2	3.4	2.874
S21(dB)	17.04	9.7	9.3	19	14-21	13.6	13	12.554
S11(dB)	-17.5	<-10	-22	<-15	<-10	-16.6	<-8	-23.847
S22(dB)	-22.4	<-12	--	<-10	--	-8.6	<-14	-17.479
Supply voltage(V)	1.8	1.1	--	1.2	1.8	1.4	1	1.2

V. CONCLUSION

The proposed LNA based micro strip antenna is designed and simulated using Advanced Design System (ADS). Various simulation parameters will be discussed in the following statistics, including the wave ratio, the threshold voltage (M1 / m2), standing wave ratio, the gain, the input reflection coefficient, the output reflection coefficient, the reverse isolation factor, the stability factor, noise count, supply voltage, power consumption and gate source voltage. The proposed micro strip antenna is to be fabricated using Fr4 substrate and investigated by simulation and measurements like radiation patterns, S-parameters and return loss by using ADSsoftware to improve the existing System. The proposed LNA receives a best results against all parameters, for example noise Ratio is 0.423, gain is 12.554dB, Voltage Standing Wave Ratio is 1.137 and Stability Factor is 1.4335.

REFERENCES

[1] Brandolini, M., Rossi, P., Manstretta, D., & Svelto, F. (2005). Towards multistandard mobile terminals fully integrated receiver requirements and architectures. IEEE Transactions on Microwave Theory and Techniques, 53(3), 1026–1038.

[2] Abidi, A. A. (2007). The path to the software-defined radio receiver. IEEE Journal of Solid-State Circuits, 42(5), 954–967.

[3] Mitola, J. (1995). The software radio architecture. IEEE Communications Magazine, 33(5), 26–38.

[4] Osmany, S. A., Herzel F., & Scheytt, J. C. (2009). An integrated 0.6–4.6 GHz, 5–7 GHz, 10–14 GHz, and 20–28 GHz frequency synthesizer for software-defined radio applications. In Proceedings of the IEEE bipolar/BiCMOS circuits and technology meeting (BCTM 2009), Capri, Italy (pp. 39–42).

[5] Zolfaghari, A., & Razavi, B. (2003). A low-power 2.4-GHz transmitter/receiver CMOS IC. IEEE Journal of Solid-State Circuits, 38, 177–181.

[6] Pandey, G. P., Kanauajia, B. K., Guatam, A. K., & Gupta, S. K. (2013). Ultra wideband L-strip proximity coupled slot loaded circular microstrip antenna for modern communication systems. Wireless Personal communication, 70, 139–151.

[7] Kumar, S., Kanaujia, B. K., Dwari, S., Pandey, G. P., & Singh, D. K. (2015). A miniurazation approach towards 40 GHz single chip receiver system for MMW Communication networks. Wireless Personal Communication. doi:10.1007/s11277-015-2688-4.

[8] Bevilacqua, A., & Niknejad, A. M. (2004). An ultrawideband CMOS low noise amplifier for 3.1–10.6- GHz wireless receivers. IEEE Journal of Solid-State Circuits, 39(12), 2259–2268.

[9] Lin, Y. J., Hsu, S. S. H., Jin, J. D., & Chan, C. Y. (2007). A 3.1–10.6 GHz ultrawideband CMOS low noise amplifier with current-reused technique. IEEE Microwave Wireless Compon. Lett., 17(3), 232–234.

[10] Vecchi, F. (2010). A wideband mm-wave CMOS receiver for Gb/s communications employing interstage coupled resonator. In Proceedings of the IEEE international solid-state conference (pp. 220–221).

[11] El-Nozahi, M., Sanchez-Sinencio, E., & Entesari, K. (2010). A millimeterwave (23–32 GHz) wideband BiCMOS low-noise amplifier. IEEE Journal of Solid-State Circuits, 45(2), 289–299.

[12] Lo, Y. T., & Kiang, J. F. (2011). Design of wideband LNAs using parallel to series resonant matching network between common-Gate and common-source stage. IEEE Transactions on Microwave Theory and Techniques, 59(9), 2285–2293.

[13] Bories, S., Pelissier, M., Delaveaud, C., & Bourtoutian, R. (2007). Performances Analysis of LNA antenna co-design for UWB system. Antennas and Propagation EuCAP, 34, 1–5.

[14] Shaeffer, D. K., & Lee, T. H. (1997). A 1.5-V, 1.5-GHz CMOS low noise amplifier. IEEE Journal of Solid-State Circuits, 32, 745–759.

[15] Allstot, D. J., Li X., & Shekhar, S. (2004). Design considerations for CMOS low-noise ampliifers. In Proceedings of the IEEE radio frequency integrated circuits (RFIC) symposium (pp. 97–100).

@IJMTER-2020, All rights Reserved