Scientific Journal Impact Factor (SJIF) : 4.364
International Journal of Modern Trends in Engineering and Research
ISSN (ONLINE) : 2349 - 9745 ISSN (PRINT) : 2393 - 8161

ENHANCED Z-SOURCE INVERTER WITH CAPACITOR VOLTAGE STRESS AND SOFT-START CAPABILITY

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Abstract- This paper proposes an improved Z-source inverter topology. Compared to the traditional Z-source inverter, it can reduce the Z-source capacitor voltage stress significantly to perform the same voltage boost, and has inherent limitation to inrush current at startup. The control strategy of the proposed Z-source inverter is exactly the same as the traditional one, so all the existing control strategy can be used directly. A soft-start strategy is also proposed to suppress the inrush surge and the resonance of Z-source capacitors and inductors. The operation principle of the proposed topology and comparison with the traditional topology are analyzed in detail. Simulation and experimental results are given to demonstrate the new features of the improved topology.
Keywords- Inrush current, soft start, Z-source inverter.

I. INTRODUCTION

The voltage-source inverter and current-source inverter are two types of traditional power inverter topology. For the voltage-source inverter fed from a voltage source, the ac output voltage is lower than the available dc bus voltage; thus, it can only perform the buck dc–ac power conversion. For the current source inverter fed from a current source, the ac output voltage, however, is greater than the dc source voltage, thus presenting a voltage boost dc–ac power conversion. In applications where both voltage buck and boost are required, an additional dc–dc converter is needed in both voltage-source and current-source inverters, which increases the system complexity and cost to a significant extent. A Z-source inverter is proposed as the single-stage inverter topology to demonstrate both buck and boost power conversion ability [1]. In addition, the two switches in the same phase leg can be gated on simultaneously and no dead time is needed, so the output distortion is greatly reduced and the reliability can be improved. Recent research on Z-source inverters mainly focuses on the modulation strategy [2]–[5], the modeling and controller design [6]–[8], the application fields [9]–[11], and other derived Z-source converter topologies [12], [13]. Despite the aforementioned merits, the traditional Z-source inverter topology also shows the following drawbacks: 1) the voltage across Z-source capacitors is no less than input voltage, thus high-voltage capacitors should be used, which may result in larger volume and prove to be cost expensive to the system; 2) it cannot suppress the inrush current and the resonance introduced by Z-source capacitors and inductors at startup, thus causing the voltage and current surge, which, in turn, may destroy the devices. To solve the aforesaid drawbacks in traditional Z-source inverter, a new Z-source inverter topology is presented with reduced Z-source capacitor voltage stress and inherent inrush current limitation at startup. It can suppress the resonance well by adopting a proper soft-start strategy. The operation principle and comparison with the traditional topology reveal the merits of the proposed topology, and are also verified in both Saber simulation and experiment.

II. CONSIDERATIONS ON Z-SOURCE INVERTER

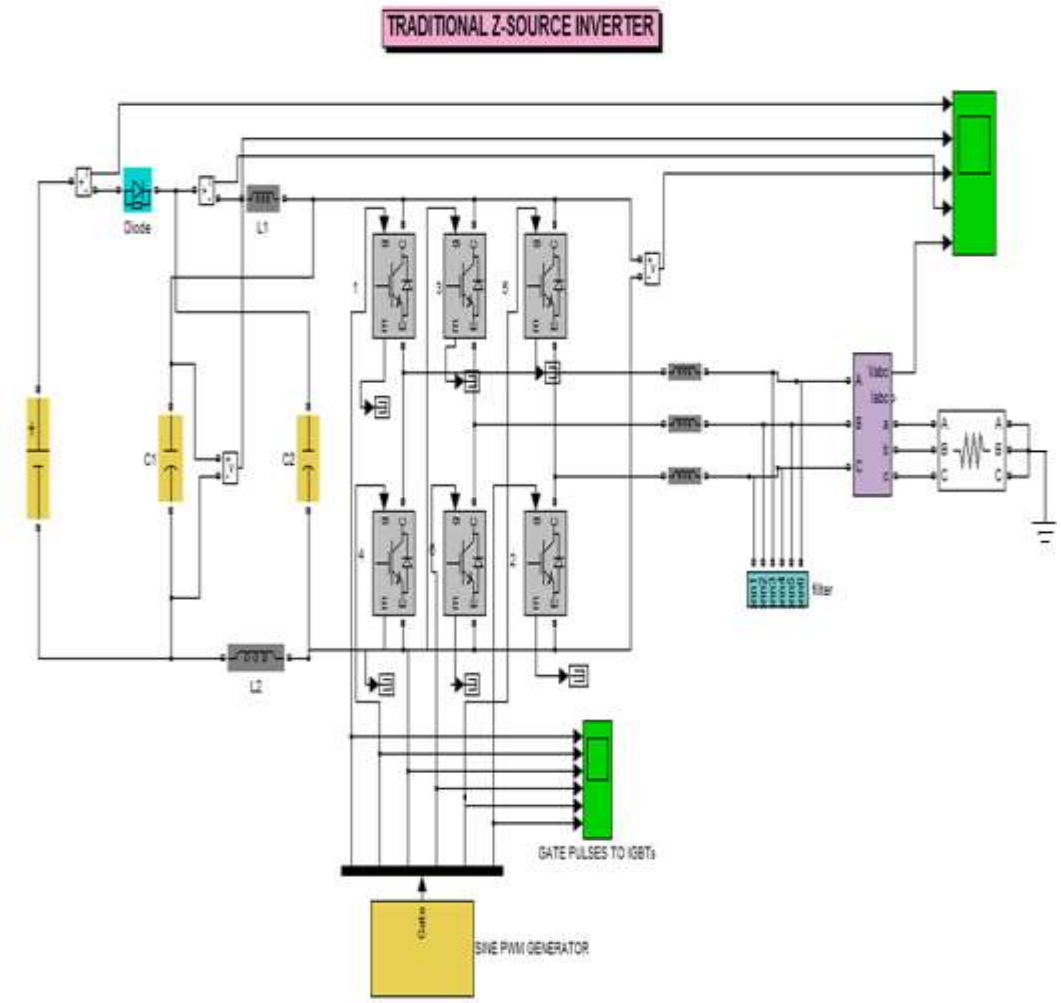


Fig. 1. Z-source inverter.

Fig. 1 shows the Z-source inverter topology where a unique impedance network is introduced to couple the inverter main circuit to the power source. The two-port impedance network consists of two identical inductors $L1$ and $L2$ and two identical capacitors C_1 and C_2 connected in X shape. The Z-source inverter has an additional shoot-through zero state, which is forbidden in voltage-source inverter. When the input voltage is high enough to produce the desired output voltage, the shoot-through zero state is not used and the Z-source inverter performs the buck conversion the same way as the voltage-source inverter. When the input voltage is low, the shoot-through zero state is used to boost the voltage; therefore, the Z-source inverter performs as a buck–boost inverter.

A. Z-Source Capacitor Voltage Stress

As described by Peng [1], the peak dc-link voltage can be expressed as

$$V_{PN} = BV_0 = \frac{1}{1-2D0}V_0. \qquad (1)$$

Where V_0 is the input dc voltage, and
B is the boost factor; B is determined by the shoot-through duty ratio D_0. The Z-source capacitor voltage is determined by

$$V_{C1} = V_{C2} = V_C = \frac{1 - D_0}{1 - 2D_O} V_0. \qquad (2)$$

As can be derived from (2), V_C is no less than V_0, thus presenting a high Z-source capacitor voltage stress.

B. Inrush Current at Startup

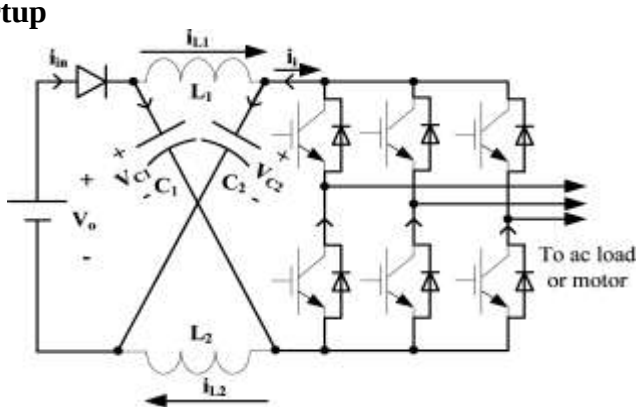


Fig. 2. Inrush current at startup.

Huge inrush current exists at Z-source inverter startup. The initial voltage across the Z- source capacitors is zero, so the current path can be seen in Fig. 2 and huge inrush current charges the capacitors immediately to 0.5*Vo*. Then, the resonance of Z-source capacitors and inductors starts, which results in large voltage and current surge. Because of the inherent current path at startup in this topology, it cannot achieve the soft-start capability.

III. IMPROVED Z-SOURCE INVERTER

The improved Z-source inverter is shown in Fig. 3. The elements used are exactly the same as the previous one. The difference is that the positions of the inverter bridge and diode are exchanged and their connection directions are inversed. The voltage polarity of Z-source capacitors in the proposed topology remains the same as the input

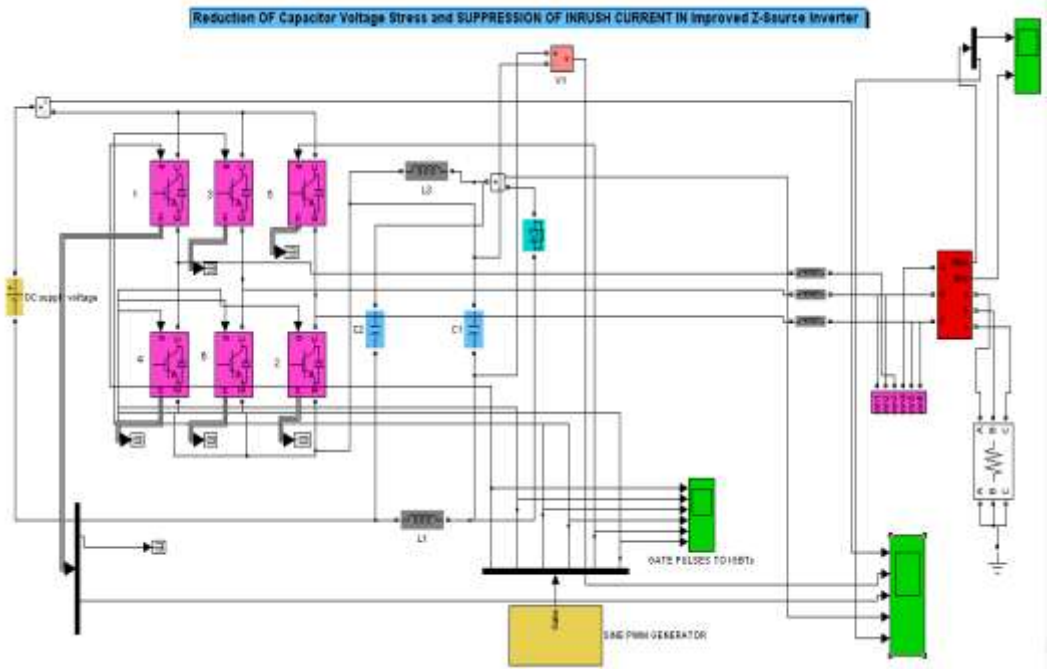


Fig. 3. Improved Z-source inverter.

voltage polarity; therefore, to get the same voltage boost, the capacitor voltage stress can be reduced to a significant extent. In addition, as can be seen from Fig.3, the topology has inherent inrush-current limitation ability compared to the previous one, because there is no current path at startup.

IV. OPERATION PRINCIPLE AND COMPARISON WITH PREVIOUS TOPOLOGY

The equivalent circuit of the improved Z-source inverter is shown in Fig. 4. Assuming that $L1 = L2 = L$, $C1 = C2 = C$, then we have

$$v_{L1} = v_{L2} = v_L, \quad V_{C1} = V_{C2} = V_C. \qquad (3)$$

When in the shoot-through state, the inverter side is shorted, as shown in Fig. 4(a), we can get

$$v_L = V_0 + V_C. \qquad (4)$$

When in the non-shoot-through state (including the active and null states), the inverter side can be simplified by an equivalent current source (the current value is zero when in null state), as shown in Fig. 4(b). The following equation can be derived in this state:

$$V_L = -V_C. \qquad (5)$$

The shoot-through duty ratio is $D0$ and the average value of vL over one switching period is zero, so we can get

$$V_C = \frac{D_0}{1 - 2D_0}. \qquad (6)$$

From this derivation, we can see that in the improved topology, when the shoot-through duty ratio $D0$ is zero, the Z-source capacitor voltage VC is equal to zero. When the converter is in the soft-starting state, VC is zero naturally, so if we control the $D0$ increase from zero gradually, VC can also increase from zero gradually and soft start can be achieved. But this is not the case in traditional topology. The peak dc-link voltage across the inverter phase legs and peak output phase voltage can be expressed as

$$V_{PN} = V_0 + 2V_C = \frac{1}{1 - 2D} V_O. \qquad (7)$$

$$V_P = M\frac{V_i}{2} = MB\frac{V_0}{2}. \qquad (8)$$

Where B is the boost factor determined by D_0 and M is the modulation ratio. As can be seen from (8), the output voltage is boosted by a factor B ($B \geq 1$), which is the same as the traditional topology.
All the power switches and diodes used in improved and traditional topologies are exactly the same. A comparison is given on the Z-source capacitor, Z-source inductor, and input current ripple.

A. Z-Source Capacitor Voltage Stress and Voltage Ripple

The peak dc-link voltage of the two topologies is exactly the same, as can be seen from (1) and (7). Comparing (6) with (2), one can see that the

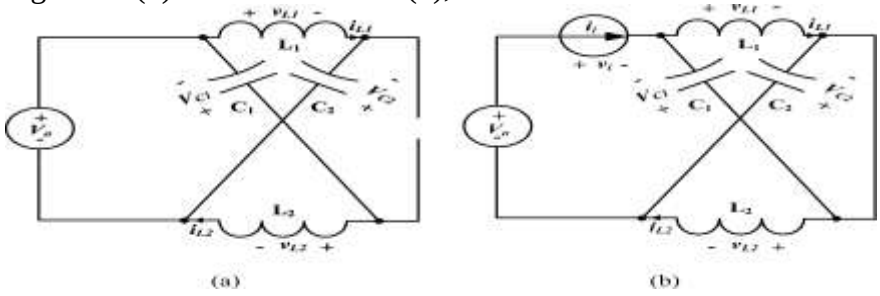


Fig. 4. Equivalent circuit of improved Z-source inverter. (a)Shoot-through state. (b) Non-shoot-through state.

Z-source capacitor voltage decreases by V_0 while maintaining the same voltage boost. The comparison of V_C in the two topologies is shown in Fig. 5.As we already know, the Z-source inverter is suitable in applications where the input voltage varies in a wide range, such as the fuel cell and photovoltaic power conditioning systems. Consider, for example, the input voltage is 150–300V. In traditional topology, the capacitor voltage stress is decided by the maximum input voltage, so V_C is no less than 300V. However, in the improved topology, *VC* is decided by the minimum input voltage to achieve the maximum voltage boost, the capacitor voltage stress is only 75V to get the required voltage boost under 150V input voltage; thus, low-voltage capacitors can be used. During shoot-through time, the condition for previous and improved Z-source inverters is the same, the Z-source inductor current discharges the capacitors; therefore, the voltage ripple across the capacitors in both inverters can be expressed as

$$\Delta V_C = \frac{I_L D_0 T}{C}. \qquad (9)$$

Where I_L is the average inductor current and T is the switching period of the Z-source network.

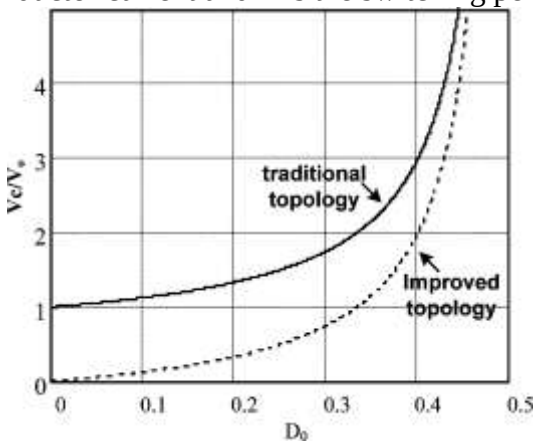


Fig. 5. V_C /V_0 versus D_0 of the two topologies.

B. Z-Source Inductor Current Ripple

The average Z-source inductor current equals the average input current; therefore, the average Z-source inductor current in both topologies is the same. For improved topology during the non-shoot-through state, as shown in Fig. 4(b), the Z-source inductor current decreases, and the current ripple can be expressed as

$$\Delta i_L = \frac{(1-D_0)TV_C}{L} = \frac{D_0(1-D_0)TV_0}{(1-2D_0)L}. \qquad (10)$$

For the previous topology, however, during the shoot-through state, the Z-source inductor current increases, and the current ripple can be expressed as

$$\Delta i_L = \frac{D_0 TV_C}{L} = \frac{D_0(1-D_0)TV_O}{(1-2D_0)L}. \qquad (11)$$

From (10) and (11), we can see that the current ripple is the same in these two topologies.

C. Input Current Ripple

The input current for a Z-source inverter is different under different controls, and the following analysis will take the simple boost control as an example. For traditional Z-source inverters, the current to the inverter bridge is i_i, so the input current can be expressed as

$$i_{in} = 2i_L - i_1. \qquad (12)$$

In shoot-through state, the input current is zero; in traditional zero-state, i_i is zero, so i_{in} is $2i_L$; in active states 1 and 2, ii is i_1 and i_2, respectively, so i_{in} is $2i_L - i_1$ and $2i_L - i_2$, respectively, and the average input current is I_L. Ignoring the inductor current ripple, i_L can be represented as I_L. The input current for traditional topology is shown in detail in Fig. 6. The deviation of input current and its average value can be expressed as

$$\Delta i_{in} = |i_{in} - I_L| = |2I_L - i_i - I_L| = |I_L - i_i|. \quad (13)$$

For improved topology, the input current is actually the current fed to the inverter bridge, so in shoot-through state, the input current is $2i_L$; in traditional zero state, the input current is zero; in active states 1 and 2, the input current is i_1 and i_2 , respectively, and the averaged input current is I_L .

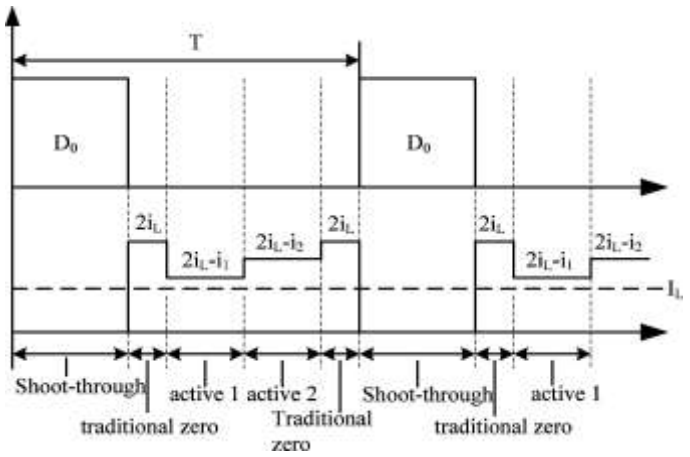


Fig. 6. Input current of the traditional Z-source inverter.

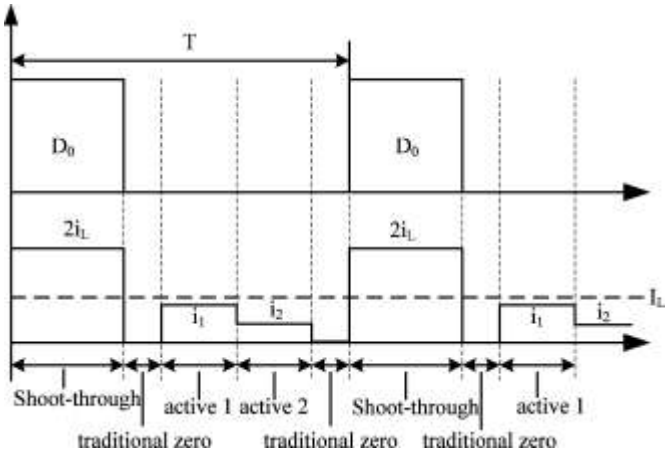


Fig. 7. Input current of the improved Z-source inverter.

The input current for improved topology is shown in detail in Fig. 7. The deviation of input current and its average value can be expressed as

$$\Delta i_{in} = |i_{in} - I_L| = |i_i - I_L|. \quad 14)$$

From (13) and (14), we can see that the input current ripple of these two topologies is exactly same.

V. SIMULATION RESULTS

The Saber simulation results are given to verify the merits of the proposed Z-source inverter and compare with the traditional one in a stand-alone system. Simple boost control is applied as an example. The simulation parameters are:

1) *Z-source network*: $L1 = L2 = 1000\ \mu$H, $C1 = C2 = 2000\ \mu$F;
2) *Output filters*: $L_f = 1000\ \mu$H, $C_f = 15\mu$F;
3) switching frequency: 20 kHz;
4) *Load*: three-phase resistance load $R = 13\Omega$/phase.

Three cases are given under different input voltages; shoot through duty ratios, and modulation ratios, while the output phase voltage is 115V in all the cases.

Case 1: $V_0 = 210$V, $D_0 = 0.218$, $M = 0.9$ with 1/6 third harmonic injection. Fig. 8(a) and (b) shows the simulation results of traditional topology and improved topology, respectively. The waveforms from top to bottom are input current i_{in} , Z-source capacitor voltage V_C, dc-link voltage V_{PN}, Z-source inductor current I_L, and output phase voltage *v*load, respectively. From

Fig. 8(a), we can see that in traditional topology, V_C is boosted to 288V in steady state, V_{PN} is boosted to 368V, and huge inrush current occurs at startup. V_C is charged from 0 to 105V instantaneously. Then, the resonance of Z-source capacitors and inductors starts, and voltage surge and current surge may destroy the converter.

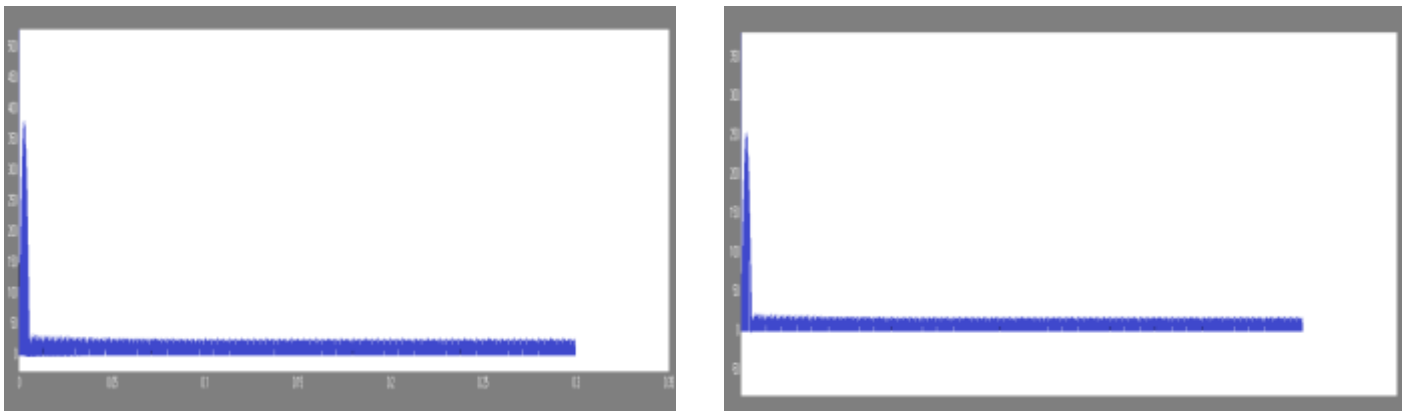
From Fig. 8(b), we can see that in improved topology, V_C is equal to 78V in steady state, V_{PN} is boosted to 368V, and the inrush current and the resonance also exist though they are much smaller than the previous one.

Case 2: $V_0 = 260$V, $D_0 = 0.187$, $M = 0.813$ without third harmonic injection. Fig. 9(a) and (b) shows the simulation results of traditional topology and improved topology, respectively.

In Fig. 9(a), we can see that in traditional topology, V_C is boosted to 335V in steady state, V_{PN} is boosted to 413V, and huge inrush current occurs at startup. V_C is charged from 0 to 130V instantaneously, and the voltage surge and current surge may also destroy the converter.

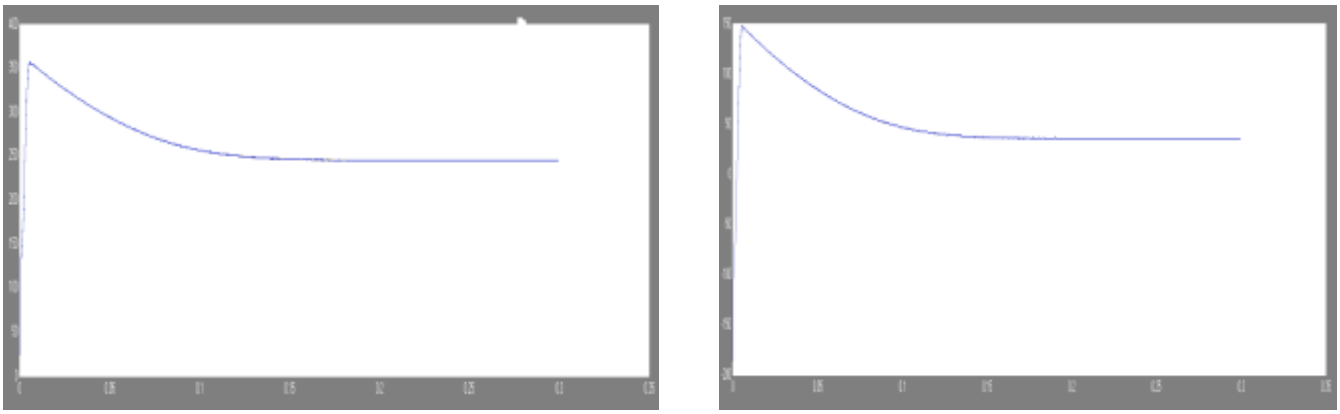
In Fig. 9(b), we can see that in improved topology, V_C is equal to 75V in steady state, V_{PN} is boosted to 413V, and the inrush current and the voltage and current surge also exist though smaller than the previous one.

Case 3: $V_0 = 320$V, $D_0 = 0$, $M = 1.05$ with 1/6 third harmonic injection. Fig. 10(a) and (b) shows the simulation results of traditional and improved topology, respectively. In Fig. 10(a), we can see that in traditional



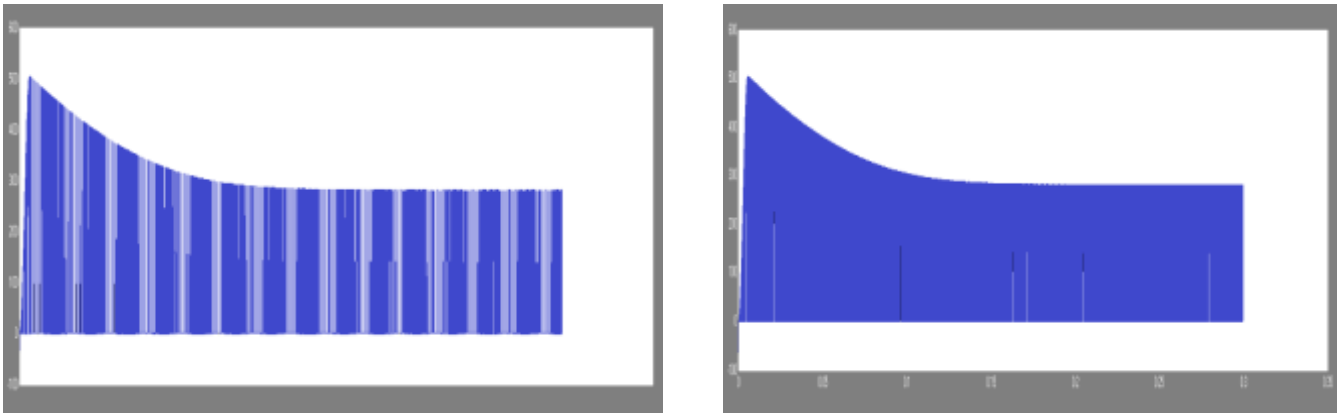
(a) (b)

Fig. 8. Simulation results in case 1. (a) Traditional topology. (b) Improved topology.



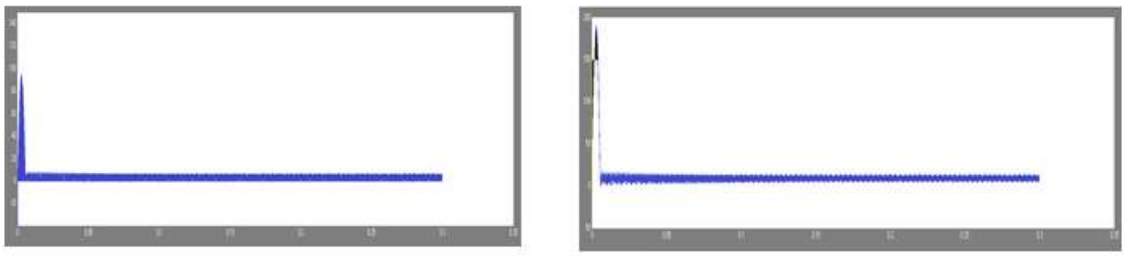
(a) (b)

Fig. 9. Simulation results in case 2. (a) Traditional topology. (b) Improved topology.



(a) (b)

Fig. 10. Simulation results in case 3. (a) Traditional topology. (b) Improved topology



(b) (C)

Fig. 11. Simulation results in case 2. (a) Traditional topology. (b) Improved topology

topology, V_C and V_{PN} are equal to V_0 in steady state, and huge inrush current occurs at startup. V_C is charged from 0 to 160V instantaneously, and the voltage surge and current surge can also be seen.

In Fig. 10(b), we can see that in improved topology, V_C is about 0V and V_{PN} is equal to V_0 in steady state, the inrush current and the resonance are well suppressed; therefore, the new topology is more reliable. Noting that there is a small negative offset across the Z-source capacitor mainly caused by the forward voltage drop of the diode, a film capacitor is more reasonable in practical use to suffer the high current ripple in the Z-source network; therefore, this negative offset is not a problem.

To avoid the resonance in improved topology, a soft-start strategy is also given here, i.e., increase D_0 from 0 gradually at startup. Fig. 11 shows the waveforms of improved topology with a soft-start strategy in case 2. D_0 increases from 0 to 0.187 in 200 ms, and we can see that the inrush current and resonance are suppressed without voltage and current surge.

VII. CONCLUSION

The proposed ZSI inherits all the advantages of the ZSI and features its unique merits. It can realize buck/boost power conversion in a single stage with a wide range of gain that is suited well for application in PV power generation systems.

The Z-source capacitor voltage stress is reduced greatly to perform the same boost ability. thus, low voltage capacitor can be utilized to reduce the system cost and volume

TRADITIONAL Z- SOURCE INVERTER

INPUT VOLTAGE(Vo)	DUTY RATIO(Do)	MODULATION INDEX(M)	CAPACITOR VOLTAGE(Vc)	DC LINK VOLTAGE(Vpn)
210V	0.218	0.9	245V	280V
320V	0	1.05	323V	328V

IMPROVED Z-SOURCE INVERTER

INPUT VOLTAGE(Vo)	DUTY RATIO(Do)	MODULATION INDEX(M)	CAPACITOR VOLTAGE(Vc)	DC LINK VOLTAGE(Vpn)
210V	0.218	0.9	35V	280V
320V	0	1.05	3V	328V

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