

## “High Frequency CMOS Amplifier with Reduced Non-Linearity”

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**Abstract-** Microwave high power amplifier (HPA) is a main device of wireless systems at the transmitter. It is responsible to increase the power level of the input signal up to certain level necessary for the transmission purposes at higher frequencies. Most of the amplifiers having the property of attenuating and distorting the signals that are required to increase the power level of the input signal. Many new methods have been proposed in recent years to achieve different levels of linearity and efficiency but the drawback was complex circuitry and trade-off between gain and bandwidth. The new technique called negative impedance compensation is introduced in this research for enhancing the linearity and power efficiency of the power amplifier without compromising gain and bandwidth. Feedback amplifier is introduced with main amplifier and the negative impedance is added to the input terminals of the main amplifier and it is analysed by using volterra model. Feedback amplifier and main amplifier is having same structure; hence the complexity of the circuit is reduced. Negative impedance is added to cancel harmonic and intermodulation distortion. Linearity is measured by plotting gain v/s frequency with and without feedback amplifier. Harmonic and intermodulation distortion is measured with and without feedback amplifier.

### I. INTRODUCTION

Microwave high power amplifier (HPA) is a main device of wireless systems at the transmitter. It is responsible to increase the power level of the input signal up to certain level necessary for the transmission purposes at higher frequencies. Linearity, stability and power efficiency of microwave HPAs are the three main parameters taken into consideration for designing the high power amplifier. [1]

Most of the amplifiers having the property of attenuating and distorting the signals that are required to increase the power level of the input signal. The presence of distortion is caused by the non-linearity of the amplifiers. The harmonic contents and the intermodulation products of output signal give measure of the level of non-linearity. [2]

The quick and high development in wireless technology has put an eminent utilization of various balances methods for example, OFDM, CDMA and QAM and so on. These methods require high linearity regarding spectral leakage and intermodulation distortion (IMD). Some new techniques have been accounted for as of late to accomplish distinctive levels of linearity by utilizing special pre-distortion, remunerating pre-post-twisting impact or consonant/intermodulation injection. These techniques concentrate on diminishing the bending at the source end, making them more efficient than the conventional linearization procedures. Be that as it may, most existing procedures typically require complex hardware, which is not reasonable for practical realization. Moreover, a few strategies may corrupt the level of linearity and efficiency when working at high working frequencies. [3]

A novel high linear amplifier technique based on the negative impedance compensation is connected to a useful circuit outline that can be used for current RF CMOS technology. [4] By utilizing the Volterra model, the particular feedback structure of the proposed linearization technique will enhance the gain and linearity moreover bandwidth also. This method is required to remove the constraints of some conventional strategies in which the linearity is enhanced by exchanging off the gain and bandwidth. [5]

## II. EXPERIMENTAL DETAILS

- i. Feedback amplifier is introduced with main amplifier and it is analysed by using volterra model.
- ii. Negative impedance is added to amplifier input terminals to cancel harmonic distortion and inter-modulation distortion.
- iii. After adding negative impedance to the input terminals of the main amplifier, the analysis is done by volterra series model.
- iv. Harmonic distortion and inter-modulation distortion are measured with and without feedback amplifier.
- v. Linearity is measured by plotting gain v/s frequency with and without feedback amplifier.
- vi. Since the feedback is positive, stability analysis is performed.
- vii. 1- dB compression point is measured with and without feedback amplifier to get the information about power efficiency.
- viii. Single chip amplifier design and test by using Virtuoso spectreRF software.

Multi-gated transistors, MIM capacitors, spiral inductors and poly resistors are used for CMOS implementation as shown in figure 2.1.

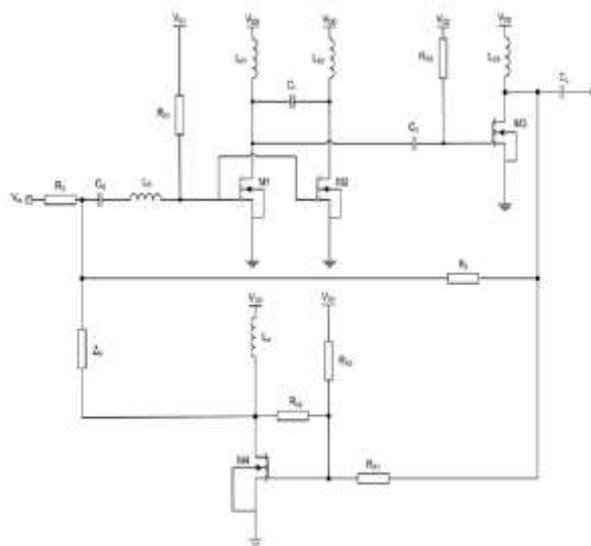


Figure 2.1 CMOS amplifier with negative impedance recompense

## III. RESULTS AND DISCUSSIONS

### 3.1 Linearity analysis

The linearity analysis of an amplifier without feedback amplifier is shown in figure 3.1.

The input is sinusoidal with ac magnitude 0.9 mv, frequency of 1.4 GHz, frequency sweep is from 1 GHz to 2 GHz

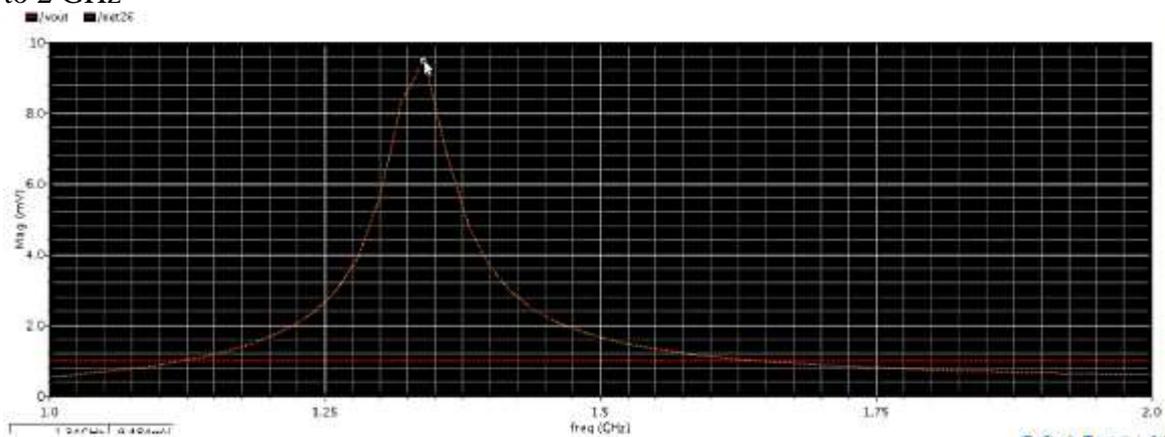


Figure 3.1 Ac response of an amplifier without feedback amplifier.

The amplifier working at frequency 1.342 GHz.  
The magnitude is 9.494 mv.  
Gain= (9.494/0.9)= 10.54.  
Bandwidth= 35.72 MHz

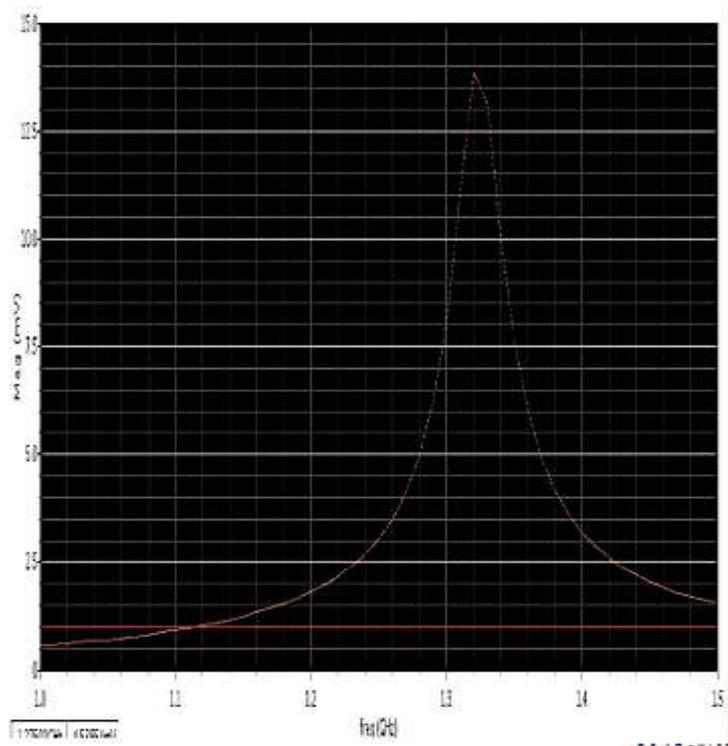


Figure 3.2 Ac response of an amplifier with feedback amplifier

The linearity analysis of an amplifier with feedback amplifier as shown in figure 3.2.

The input is sinusoidal with ac magnitude 0.9 mv, frequency of 1.4 GHz, frequency sweep is from 1 GHz to 1.5 GHz

The amplifier working at frequency 1.334 GHz.

The magnitude is 13.742 mv.

Gain= (13.742/0.9)= 15.26.

Bandwidth= 35.96 MHz

From the analysis of both feedback amplifier and without feedback amplifier, the linearity is increased with feedback amplifier because adding negative impedance to the input terminals gives positive feedback to whole circuit, hence gain is increased.

The bandwidth of feedback amplifier and without feedback amplifier is almost same, hence the gain is increased without compromising bandwidth.

Linearity improvement=  $\frac{13.742-9.494}{9.494} = 44.74\%$ .

### 3.2 Distortion analysis

Procedure for distortion analysis in cadence spectreRF

- Change the Input Port Parameters in Schematic Window  
50 Ohms in Resistance  
1 in Port Number  
Sine in Source Type  
Frf1 in Frequency name 1 field  
Frf in Frequency 1 field  
Prf in Amplitude1 (dBm) field  
Check and save the schematic
- Verify the variable values in the ADE window  
Frf = 1.4 GHz

Prf = -20dBm

- In the ADE window, select Analysis\_ Choose
- The Choose Analysis window shows up  
Select pss for Analysis  
In Fundamental Tones section, the following line should be visible  
1 frf1 frf 1.4G Large PORT1  
Check the Auto Calculate Box  
Beat Frequency → 1.4G (Automatically appears)  
No of Harmonics → 20  
Accuracy Default → Moderate  
Enable Box in the bottom should be checked.  
Click OK
- In the ADE window click on Simulation → Netlist and Run to start the simulation make sure that simulation completes without errors.
- In the ADE window, select Results → Direct Plot → Main Form
- The analysis choose window shows up  
Select PSS for analysis  
Select Function as Voltage Gain  
Modifier → dB20, Input Harmonics → 1.4G  
Select → Output and then activate the schematic window and select RF\_OUT;  
Select → Input then activate the schematic window and select RF\_IN  
At the top of PSS result window change the plot mode to append.  
Now Select Function as Voltage  
Sweep → Spectrum, Signal Level → peak, Modifier → dB20  
Select → net and then point to RF\_OUT net in schematic the results are plotted.

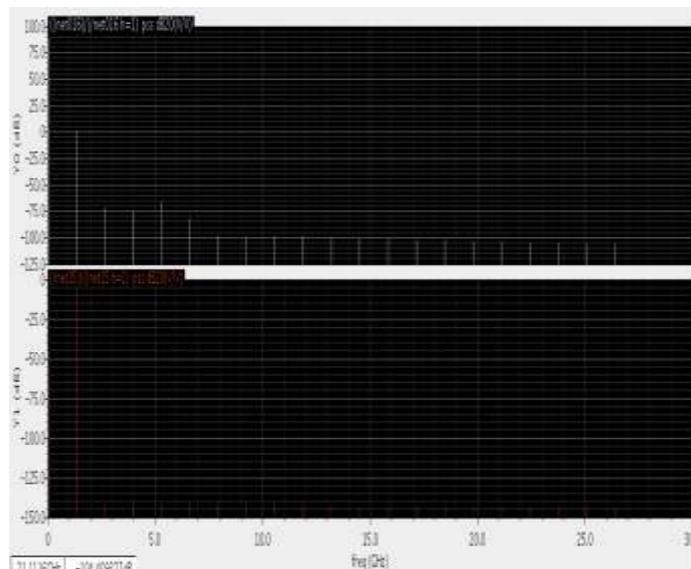


Figure 3.3 Harmonic distortion without feedback amplifier.

The harmonic distortion analysis by using 20 harmonics at beat frequency of 1.4 GHz is shown in figure 3.3.

#### IV. CONCLUSION

The trade-off between the gain and bandwidth of the power amplifier leads to introduce the new technique called the negative impedance compensation. This technique increases the linearity without the compromise of gain and bandwidth. Adding negative impedance to the input terminal of an amplifier and introducing feedback amplifier to the circuit reduces harmonic and inter-modulation

distortion. Linearity is measured by considering feedback amplifier and without feedback amplifier. Feedback amplifier and negative impedance give rise to positive feedback, hence gain is increased with feedback amplifier. Linearity is increased by 44.74% and bandwidth remains almost constant and the value is 35.62 MHz. Harmonic distortion is measured by considering feedback amplifier and without feedback amplifier. The number of harmonics present without feedback amplifier is more compared with feedback amplifier and the amplitude of harmonics present in the second and third order harmonics are less with feedback amplifier. Harmonic distortion cancellation is better with negative impedance and feedback amplifier. 1-dB compression point is plotted with and without feedback amplifier. The input power level is more for an amplifier with feedback, hence the 1-dB gain drop due to power level occurs at high signal power level compared with an amplifier without feedback. This increased the power efficiency of the power amplifier

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