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A COMPARATIVE ANALYSIS OF 13 AND 15 LEVEL H-BRIDGE MULTI LEVEL INVERTERS

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Abstract- As the power demand is increasing continuously, the use of nonconventional sources is rapidly increasing. Among the different non-conventional energy sources, solar energy is finding more applications because it is freely and abundantly available in nature. The Solar energy is converted into electricity using PV modules whose output is generally DC in nature and is required to be converted into AC with the use of inverters. As Compared to two level inverters, multilevel inverters give better output. In multilevel inverters as the number of levels in the output voltage increase, the accuracy of the system increases and the output voltage gets approached near to the sinusoidal [2]. However, as the levels in multilevel inverter increases the complexity of the control system increases and the control strategy required becomes much complicated. With the increment of number of levels, the number of switches also increases so the system losses also increase linearly. So at every stage user has to make a trade off with the quality of the output and complexity of the circuit [3]. In this paper the authors have considered 13 and 15 levels of H-bridge cascaded inverters and carried out the simulation studies using MATLAB/Simulink software, with equal angle switching and equal area switching methods for different levels of inverters. A comparative study with different parameters of the multilevel inverters is performed for the selection of required levels in multilevel inverter.

Keywords - Multilevel inverter, MATLAB/*Simulink*, equal angle method, equal area method, and THD.

I. INTRODUCTION

As the cost of fossil fuels continue to rise, other sources of energies are becoming important. Renewable energy sources (solar, wind, fuel cell etc.) are considered as alternative energy sources to conventional fossil fuel energy sources due to environmental pollution and global warming problems[5]. *Solar energy* is one of the most promising renewable sources that can be used to produce electric energy through photovoltaic (PV) process. A significant advantage of PV system is the use of abundant and free energy from the sun. However, these systems still face major challenges that limit their widespread use due to their high cost and low efficiency when compared with other renewable technologies. Moreover, the intermittent nature of the output power of PV systems reduces their reliability in providing continuous power to customers [6]. In addition, the fluctuations in the output power due to variations in irradiance and presence of harmonics might lead to undesirable performance of the electric network. Grid-connected PV-Systems consist of three main blocks: DC bus (PV panels), power converter and electrical network. The power converter acts as an interface between the DC voltage, and AC grid, injecting power into electrical network. The DC/AC conversion is performed in this power converter introduces harmonics, some power losses such as switching losses, conduction losses and losses in reactive elements. An optimal design is needed to reduce these losses so that a reliable quality output and higher efficiency is obtained.

In comparison to hard switched two levels inverter, multilevel inverter can operate at high voltage with lower *dv/dt* [7]. There are three basic MLI topologies: Diode-clamped and flying-capacitor MLIs, requiring only one dc source, and cascaded H-bridge MLI (CHB-MLI), [2] requiring separate dc sources. The three types of multi-level inverters are explained below [1].

II. DIODE-CLAMPED INVERTER (NEUTRAL-POINT CLAMPED)

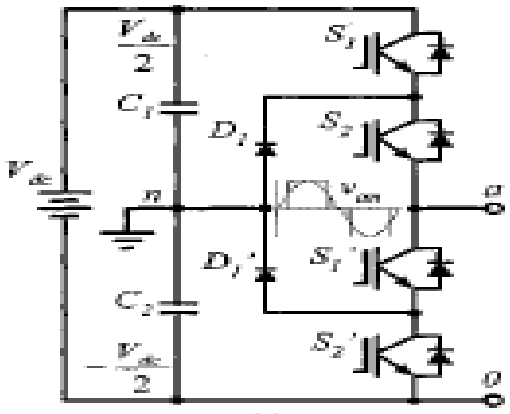

Fig1. Circuit Diagram of Three Level Diode Clamped Inverter

Figure 1 shows the diode clamped topology of three levels multilevel inverter. The key components that distinguish this circuit from a conventional two-level inverter is D_1 and D_1'. These two diodes clamp the switch voltage to half the level of the dc-bus voltage. As we can see that there are four switches present in the circuit and input voltage is divided in two parts with two diodes D_1 and D_1'. The output voltage V_{an} has three voltage states are $+V_{dc}/2$, $-V_{dc}/2$, 0. For $+V_{dc}/2$ switches S_1 and S_2 will operate, for $-V_{dc}/2$ switches S_1' and S_2' will operate and for 0 level S_2 and S_1' need to operate. The number of diodes required can be given by following equation:

$$N = (M-1) \times (M-2) \qquad [1]$$

Where,

N= number of diodes

M= number of levels at inverter output

Here, in this case if we put M = 3 then the number of diodes required would be N=2. For an example if we take 15 level inverter, then the number of diodes required from above equation would be 182. It is clear from above example that as we go for higher levels the number of diodes required will be very large. So due to stated drawback diode clamped inverter topology is rarely used for higher levels.

III. CAPACITOR CLAMPED INVERTER

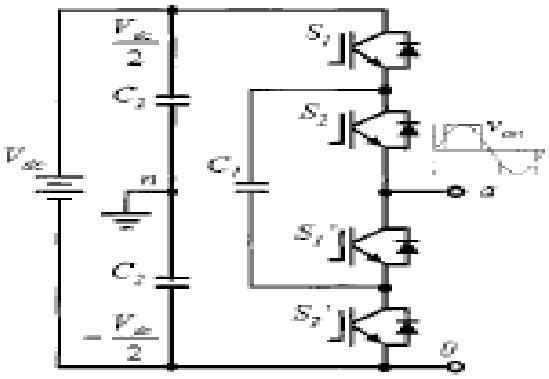

Fig 2. Circuit diagram of capacitor clamped multilevel inverter

In figure 2, a circuit diagram of capacitor clamped three levels multilevel inverter is shown. The key components that distinguish this circuit from a conventional two-level inverter is C_1. The capacitor C_1 clamp the switch voltage to half the level of the dc-bus voltage. As we can see that there are four switches present in the circuit and input voltage is divided in two parts with the capacitor presentC_1. The output voltage V_{an} has three voltage levels and they are $+V_{dc}/2$, $-V_{dc}/2$, 0. For $+V_{dc}/2$. The Switches S_1 and S_2 will operate, for $-V_{dc}/2$ switches S_1' and S_2' will operate and for 0

level either pair (S_1S_1')or (S_2S_2') can operate. The number of capacitors required can be given by following equation:

$$N = ((M-1) \times (M-2))/2 \quad [2]$$

Where,

N= number of capacitors

M= number of levels at inverter output

According to the above equation (2), for M= 3 the number of capacitors required would be 1.For an example if we take M=15 the number of capacitors required will be 91, which is significantly high. Though it is lesser than the diode clamped topology but practically it will be difficult to use so many number s capacitors. In addition to these capacitors ($M-1$) main dc bus capacitors are also required.

IV. CASCADED H-BRIDGE INVERTER

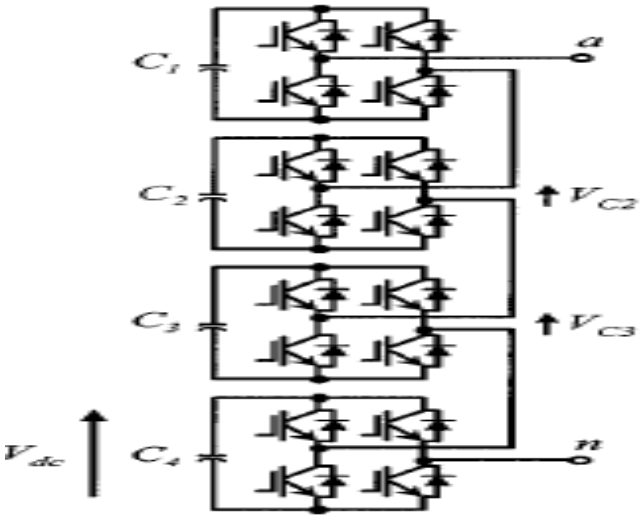

Fig 3. Cascaded H bridge multilevel inverter

In figure 3 cascaded H -bridge multilevel inverter topology for N level inverter is shown. The output level and number of H-Bridges required are related by the equation,

$$M = (2N+1) \quad [3]$$

Where,

N= number of H-bridges

M= number of levels at inverter output

As an example to get 15 levels at the output, 7 H- Bridges are required. This corresponds to 28 power devices, which is fewer compared to the diode and capacitor clamped topologies. The Cascaded H-Bridge inverter uses a separate DC source for each bridge. This becomes a very attractive feature in the case of PV systems, because solar cells can be assembled in a number of separate DC sources. Since their output voltage is a modulated staircase, they outperform two-level PWM inverters in terms of total harmonic distortion (THD), without the use of bulky expensive and dissipative passive filters. Therefore, recently, they have been finding more applications in field of solar energy power conversion systems. If there is increment in the output levels, then the waveform becomes more sinusoidal and % THD content decreases. This will increase the quality of the output signal. On the other hand, with the increment in the output levels, the number of H-Bridges required also increases and. this results in more number of switches. Hence, the complexity of the switching circuit increases. Further, rise in number of switches leads to higher switching losses, decrement in the efficiency and increment in the cost by making the circuit bulky. So the user has to make a trade off with the quality of the output and complexity of the circuit. Here in this paper the authors have

considered 13 and 15 levels of H Bridge cascaded inverters and have made simulation studies using MATLAB/ Simulink software, with equal angle switching and equal area switching methods. A comparative study between different parameters of the inverters is done for the selection of required inverter. The obtained results are presented in the result section.

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4. 13 Level multilevel inverter

A 13 level inverter uses 6 H-Bridges in cascade with 6 separate DC sources. As every bridge is having 4 switches, there are total of 24 switches. The13 output voltage levels of the output voltage are $+V_{dc}, +2V_{dc}, +3V_{dc}, +4V_{dc}, +5V_{dc}, +6V_{dc}, 0, -V_{dc}, -2V_{dc}, -3V_{dc}, -4V_{dc}, -5V_{dc}, -6V_{dc}$. The 13 level H-Bridge inverter considered for */Simulink* software is given below. Here, in this paper symmetrical H-bridge topology has been used to get the 312 volts peak output voltage, with 6 separate DC source s of input voltage value 52 volts. The switching table is the switches is presented in table1.1

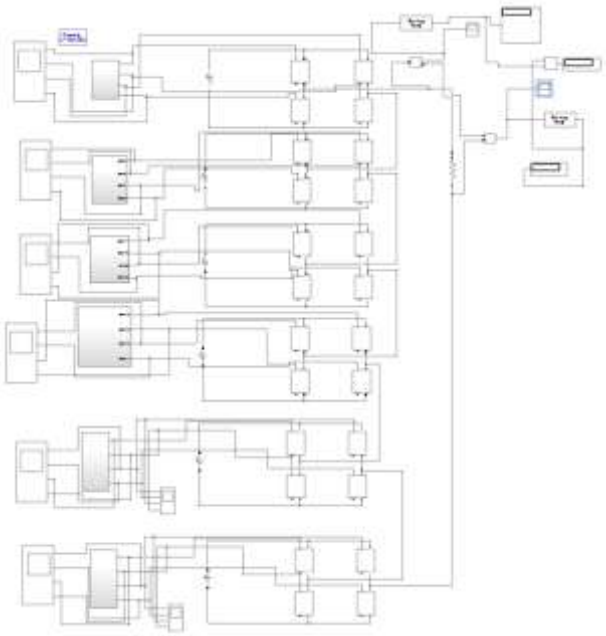


Fig 4.Simulation Circuit Diagram Of 13 Level Multilevel Inverter

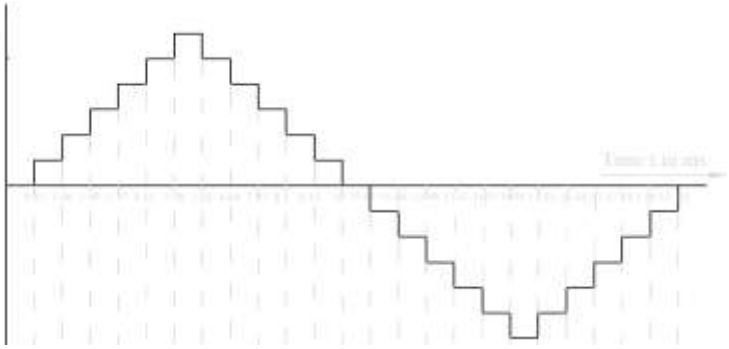


Fig 5.Waveform of 13 level multilevel inverter

LEVELS	S1	S2	S3	S4	S5	S6	S7	S8	S9	S10	S11	S12	S13	S14	S15	S16	S17	S18	S19	S20	S21	S22	S23	S24
6V	1	1	0	0	1	1	0	0	1	1	0	0	1	1	0	0	1	1	0	0	1	1	0	0
5V	1	1	0	0	1	1	0	0	1	1	0	0	1	1	0	0	1	1	0	0	0	1	0	0
4V	1	1	0	0	1	1	0	0	1	1	0	0	1	1	0	0	0	1	0	0	0	1	0	0

3V	1	1	0	0	1	1	0	0	1	1	0	0	0	1	0	0	0	1	0	0	0	1	0	0
2V	1	1	0	0	1	1	0	0	0	1	0	0	0	1	0	0	0	1	0	0	0	1	0	0
1V	1	1	0	0	0	1	0	0	0	1	0	0	0	1	0	0	0	1	0	0	0	1	0	0
0V	0	0	0	1	0	0	0	1	0	0	0	1	0	0	0	1	0	0	0	1	0	0	0	1
-1V	0	0	1	1	0	0	0	1	0	0	0	1	0	0	0	1	0	0	0	1	0	0	0	1
-2V	0	0	1	1	0	0	1	1	0	0	0	1	0	0	0	1	0	0	0	1	0	0	0	1
-3V	0	0	1	1	0	0	1	1	0	0	1	1	0	0	0	1	0	0	0	1	0	0	0	1
-4V	0	0	1	1	0	0	1	1	0	0	1	1	0	0	1	1	0	0	0	1	0	0	0	1
-5V	0	0	1	1	0	0	1	1	0	0	1	1	0	0	1	1	0	0	1	1	0	0	0	1
-6V	0	0	1	1	0	0	1	1	0	0	1	1	0	0	1	1	0	0	1	1	0	0	1	1

Table 1. 13 level inverter switching table.

V. LEVEL MULTILEVEL INVERTER

A 15 level inverter uses 7 H-Bridges in cascade with 7 separate DC sources. Since every bridge is having 4 switches, there are total of 28 switches. The15 levels of the output voltages are,

$+V_{dc}$, $+2V_{dc}$, $+3V_{dc}$, $+4V_{dc}$, $+5V_{dc}$, $+6V_{dc}$, $+7V_{dc}$, 0, $-V_{dc}$, $-2V_{dc}$, $-3V_{dc}$, $-4V_{dc}$, $-5V_{dc}$, $-6V_{dc}$.$-7V_{dc}$. The 15 level H-Bridge inverter considered for *matlab/Simulink* software is given below. Here, in this paper symmetrical H-bridge topology has been used to get the 312 volts peak output voltage, with 7 separate DC sources each of input voltage value 44 volts. The switching table of the switches is presented in table1.1

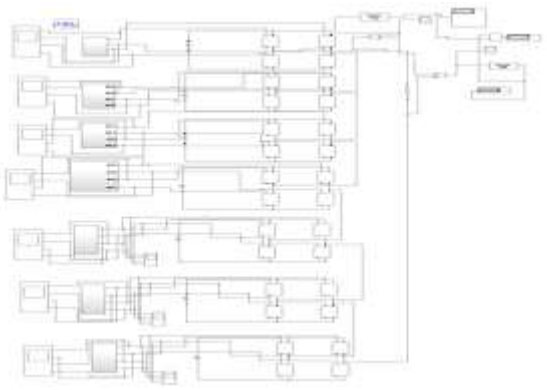


Fig 6. Simulation Circuit Diagram of 15 Level Multilevel Inverter

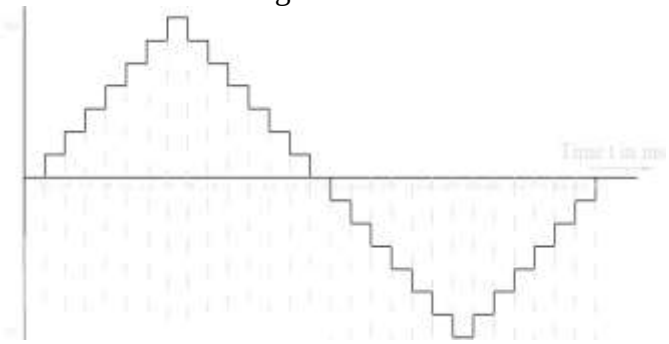


Fig 7.Waveform of 15 levels multilevel inverter

LEVELS	S1	S2	S3	S4	S5	S6	S7	S8	S9	S10	S11	S12	S13	S14	S15	S16	S17	S18	S19	S20	S21	S22	S23	S24	s25	s26	s27	s28
7V	**1**	**1**	**0**	**0**	**1**	**1**	**0**	**0**	**1**	**1**	**0**	**0**	**1**	**1**	**0**	**0**	**1**	**1**	**0**	**0**	**1**	**1**	**0**	**0**	**1**	**1**	**0**	**0**
6V	1	1	0	0	1	1	0	0	1	1	0	0	1	1	0	0	1	1	0	0	1	1	0	0	0	1	0	0
5V	1	1	0	0	1	1	0	0	1	1	0	0	1	1	0	0	1	1	0	0	0	1	0	0	0	1	0	0

4V	1	1	0	0	1	1	0	0	1	1	0	0	1	1	0	0	0	1	0	0	0	1	0	0	0	1	0	0
3V	1	1	0	0	1	1	0	0	1	1	0	0	0	1	0	0	0	1	0	0	0	1	0	0	0	1	0	0
2V	1	1	0	0	1	1	0	0	0	1	0	0	0	1	0	0	0	1	0	0	0	1	0	0	0	1	0	0
1V	1	1	0	0	0	1	0	0	0	1	0	0	0	1	0	0	0	1	0	0	0	1	0	0	0	1	0	0
0V	0	0	0	1	0	0	0	1	0	0	0	1	0	0	0	1	0	0	0	1	0	0	0	1	0	0	0	1
- 1V	0	0	1	1	0	0	0	1	0	0	0	1	0	0	0	1	0	0	0	1	0	0	0	1	0	0	0	1
-2V	0	0	1	1	0	0	1	1	0	0	0	1	0	0	0	1	0	0	0	1	0	0	0	1	0	0	0	1
-3V	0	0	1	1	0	0	1	1	0	0	1	1	0	0	0	1	0	0	0	1	0	0	0	1	0	0	0	1
-4V	0	0	1	1	0	0	1	1	0	0	1	1	0	0	1	1	0	0	0	1	0	0	0	1	0	0	0	1
-5V	0	0	1	1	0	0	1	1	0	0	1	1	0	0	1	1	0	0	1	1	0	0	0	1	0	0	0	1
-6V	0	0	1	1	0	0	1	1	0	0	1	1	0	0	1	1	0	0	1	1	0	0	1	1	0	0	0	1
-7V	0	0	1	0	0	0	1	1	0	0	1	1	0	0	1	1	0	0	1	1	0	0	1	1	0	0	1	1

Table2. 15 level inverter switching table.

VI. SIMULATION RESULTS

The simulation studies on 13 and 15 level H-Bridge inverter circuits shown in fig 6.2,6.3,7.2,7.3 has been carried out using two techniques.

1. Equal angle method: In this method conduction period of all the switches are equal. Total time is equally shared for all the levels and switches allowed to conduct for equal interval time.
2. Equal Area method: In this method, conduction period of the switches are not equal but all the level of signal will have same amplitude.

The results obtained are presented below.

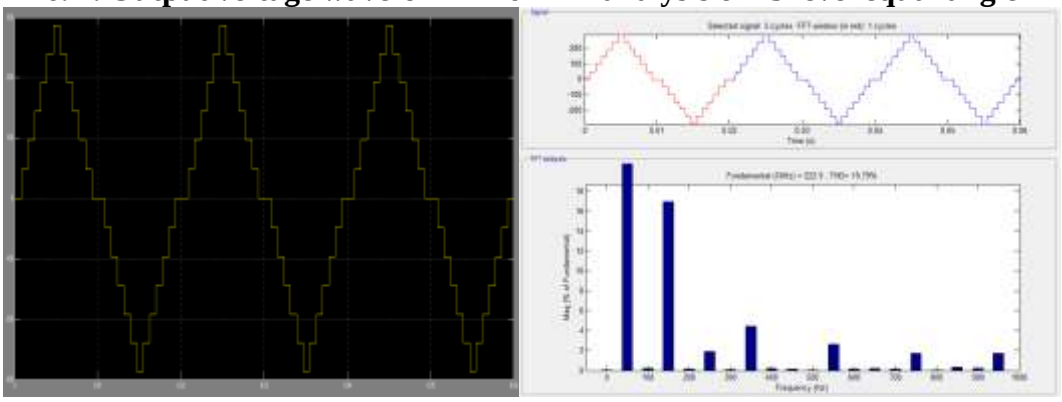
6.1 Level multilevel inverter

1. Timing Table

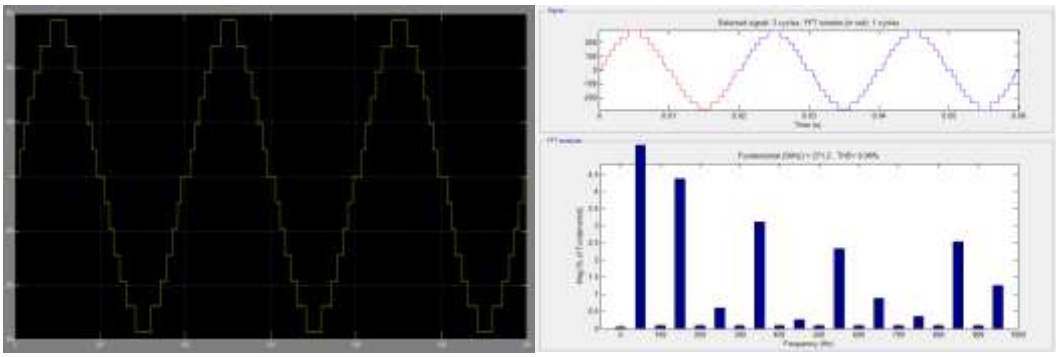
		equal angle method			equal area method		
switches		**pulse width(%)**	**Delay(msec)**	**Ton(msec)**	**pulse width(msec)**	**Delay(msec)**	**Ton(msec)**
s1		42.35	0.77	8.47	44.8685	0.5133	8.9737
s2		42.35	0.77	8.47	44.8685	0.5133	8.9737
s3		42.35	10.78	8.47	44.8685	10.5133	8.9737
s4							
	s41	3.85	0	0.77	2.5665	0	0.5133
	s42	53.9	9.24	10.78	52.565	9.487	10.513
s5		34.65	1.54	6.93	39.5955	1.0406	7.9191
s6		42.35	0.77	8.47	44.8685	0.5133	8.9737
s7		34.65	11.55	6.93	39.5955	11.0406	7.9191
s8							
	s81	3.85	0	0.77	2.5665	0	0.5133
	s82	53.9	9.24	10.78	52.565	9.487	10.513
s9		26.95	2.31	5.39	6.8071	1.5966	6.8071
s10		42.35	0.77	0.77	44.8685	0.5133	8.9737
s11		26.95	12.32	5.39	6.8571		6.8571
s12							
	s121	3.85	0	0.77	2.5665	0	0.5133
	s122	53.9	9.24	10.78	52.565	9.487	10.513

s13		19.25	3.08	3.85	27.8005	2.2201	5.5601
s14		42.35	0.77	0.77	44.8685	0.5133	8.9737
s15		19.25	13.09	3.85	27.8005	12.2201	5.5601
s16							
	s161	3.85	0	0.77	2.5665	0	0.5133
	s162	53.9	9.24	10.78	52.565	9.487	10.513
s17		11.55	3.85	2.31	20.33325	2.96685	4.81335
s18		42.35	0.77	8.47	44.8685	0.5133	8.9737
s19		11.55	13.86	2.31	20.3325	12.96685	
s20							
	s201	3.85	0	0.77	2.5665	0	0.5133
	s202	53.9	9.24	10.78	52.565	9.487	10.513
s21		3.85	4.62	0.77	8.655	4.3148	1.7311
s22		42.35	0.77	8.47	44.8685	0.5133	8.9737
s23		3.85	14.63	0.77	8.655	4.3148	1.7311
s24							
	s241	3.85	0	0.77		0	0.5133
	s142	53.9	9.24	10.78	52.565	9.487	10.513

6.2 . Output voltage waveform And FFT analysis of 13 level equal angle



6.3 Output voltage waveform And FFT analysis for Equal Area method

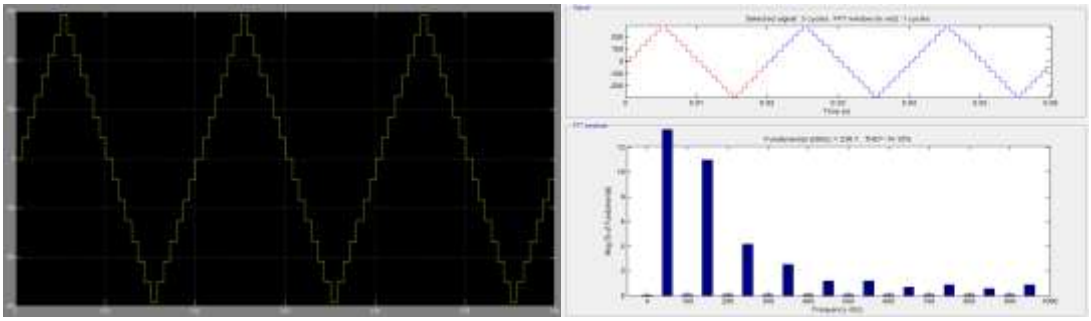


6.4 Level multilevel inverter

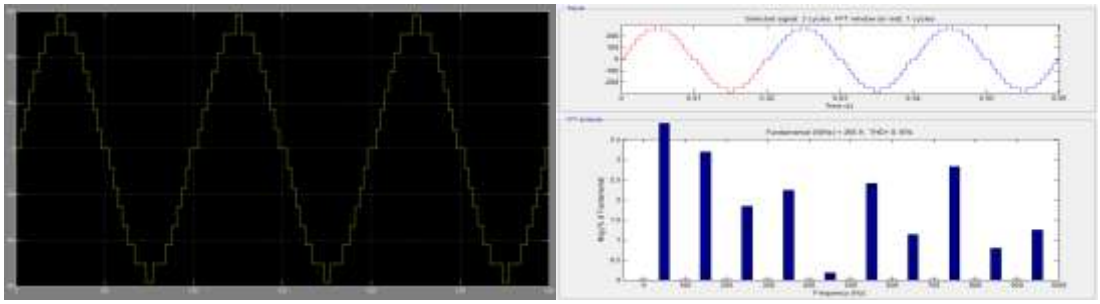
1. Timing Table

		equal angle method			equal area method		
switches		**pulse width**	**Delay(msec)**	**Ton(msec)**	**pulse width**	**Delay(msecc)**	**Ton(msec)**
s1		43.3355	0.6667	8.6667	45.4338	0.45684	9.08676

s2		43.3355	0.6667	8.6667	45.4338	0.45684	9.08676
s3		43.3355	10.6672	8.6667	45.4338	10.45684	9.08676
s4							
	s41	3.3335	0	0.6667	2.2842	0	0.45684
	s42	53.3335	9.3338	10.6667	52.282	9.5436	10.4564
s5		36.6685	1.3334	7.3337	40.76135	0.92403	8.15227
s6		43.3355	0.6667	8.6667	45.4338	0.45684	9.0876
s7		36.6685	11.3339	7.337	40.76135	10.92403	8.15227
s8							
	s81	3.3335	0	0.6667	2.2842	0	0.45684
	s82	53.3335	9.3338	10.6667	52.282	9.5436	10.4564
s9		30.0015	2.0001	6.0003	35.8735	1.9128	7.1747
s10		43.3355	0.6667	8.6667	45.4338	0.45684	9.0876
s11		30.0015	12.0006	6.0003	35.8735	11.4128	7.1747
s12							
	s121	3.3335	0	0.6667	2.2842	0	0.45684
	s122	53.3335	9.3338	10.6667	52.282	9.5436	10.4564
s13		23.3345	2.6668	4.6669	30.6175	1.9384	6.1235
s14		43.3355	0.6667	8.6667	45.4338	0.5684	9.0876
s15		23.3345	12.6673	4.6669	30.6175	11.9384	6.1235
s16							
	s161	3.3335	0	0.6667	2.2842	0	0.45684
	s162	53.3335	9.3338	10.6667	52.282	9.5436	10.4564
s17		16.66	3.3335	3.3335	24.6165	2.5385	4.9233
s18		43.3355	0.6667	8.6667	45.4338	0.5684	9.0876
s19		16.66	13.334	3.3315	24.6165	12.5385	4.9233
s20							
	s201	3.3335	0	0.6667	2.2842	0	0.45684
	s202	53.3335	9.3338	10.6667	52.282	9.5436	10.4564
s21		10.0005	4.0002	2.0001	17.154	3.2848	3.4308
s22		43.3355	0.6667	8.6667	45.4338	0.5436	9.0876
s23		10.0005	14.0007	2.0001	17.154	13.2848	3.4308
s24							
	s241	3.3335	0	0.6667		0	0.45684
	s242	53.3335	9.3338	10.6667	52.565	9.487	10.4564
s25		3.3335	4.6669	0.6667	3.9735	9.5436	0.795
s26		43.3355	0.6667	8.6667	45.43389	0.5684	9.0876
s27		3.3335	14.6674	0.6667	3.9735	14.6025	0.735
s28							
	s281	3.3335	0	0.6667	2.2842	0	0.45684
	s282	53.3335	9.3338	10.6667	52.282	9.5436	10.4564



6.5. Output Voltage Waveform and FFT Analysis For Equal Angle Method



6.6 Output voltage waveform And FFT Analysis For Equal area method

Table 3. Comparison of THD% for 13 and 15 levels

	Equal Angle Method			Equal Area Method		
Levels	THD	o/p voltage	fundamental o/p	THD	o/p voltage	fundamental o/p
13 LEVEL	15.71%	160.6	220.9	8.98%	192.5	271.2
15 LEVEL	14.12%	170.4	238.7	8.16%	189.3	266.9

VII. CONCLUSION

In this paper a single-phase multilevel cascaded H-bridge inverter for PV applications with 13 and 15 levels in the output signals are considered. Analysis and simulation has been carried out using equal area and equal angle methods with matlab/Simulink. By comparing the both the methods the results are presented in table 3. From the results derived it is clear that 15 level has lesser THD as compared to 13 level and also equal area method gives better output as compared to equal angle method. From the results it can be concluded that as the levels in the output increased THD content reduces. The design of multi-level inverter is found to be better suited for PV systems.

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