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REVIEW OF POWER DISSIPATION REDUCTION TECHNIQUES OF LOW NOISE AMPLIFIER

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Abstract— In this paper we review and discuss the techniques that is used to reduce the reflection and content of noise in amplifier design, in the past decades many numbers of technique presented by researcher to improve the performance of amplifier. Linearity of amplifier is the important parameters to consider in the design. Linearity of amplifier design by content of reflection and noise figure of amplifier. In recent application of commercial and industry needed and preferred more stability of amplifier, this type of amplifier used in GPS, satellite communication, Bluetooth Wi-Max, radar, used in portable device like laptop, used in stabilizer. Low noise amplifier have important feature like amplify the signal with rejection of noise. Low noise amplifier in modern communication used as filter with amplifier. Recent scenario low noise amplifier available in wide band, single band, multi-band frequency of application. Low noise amplifier available with high gain, noise rejection and with less power consumption. In this paper we review the work of past decades done in low noise amplifier. Low noise amplifier products full fill all requirements of modern wireless communications. So that we review and discuss the future requirement of technology is needed to discuss. in this paper discusses issues of low noise amplifier and low power dissipation amplifier, its application, issues and recent trends, in this paper review some techniques of low noise amplifier to improve perform and surveyed almost all the possible work of past decades.

Keywords— MultipleGatedTransistor**,**Bulk-Bias Control, Gain-Enhancement Techniques, Multiband Feedback and Gain-Reuse

I. INTRODUCTION

WITH THE growing demand of complex mobile devices that can function in multi-standard wireless communication systems for various user roaming needs, multi-mode and multi-band power amplifiers (MMPAs) have become a critical component for future handset development because of their frequency flexibility, easy implementation, and small size. The MMPA adaptability enables the performance and cost constraint challenges on the reconfigurable RF front-end by reducing the number of the dedicated single-band power amplifiers (PAs) foreach additional frequency band [1]–[5]. Distributed and balanced amplifiers are the most commontechniques used for broadband applications [6]–[11]. However,the distributed amplifier topology requires a large number of transistors to obtain the constant gain, which increases cost and reduces efficiency. A balanced amplifier with a quarter-wavelength coupler has a relatively large chip size and is not practical at low gigahertz-range integrated circuits (ICs) for handset wireless communication. Another approach is implementing tunable or multi section matching networks at the output port of an MMPA [12]–[18].Although a matching network with multiple elements broadens operating bandwidth, its loss increases accordingly. For the tunable PA, the programmable output matching network with varactors or microelectromechanical systems (MEMS) switches are employed to achieve flexible load impedance [19]–[21]. The efficiency and linearity of the tunable PA are degraded by the low , restricted tuning range, and limited power-handling capability of the matching networks at the PA output port [22]–[24]. Moreover, many tunable matching networks have been implemented by off-chip devices with different processes and the sophisticated multi-chip-module packaging is required [2], [18], [25].

II. REVIEW OF TECHNIQUES

A. Adopting Multiple Gated Transistors

Highly linear receiver RF front-end adopting MOSFET transconductance linearization by linearly superposing several common-source FET transistors in parallel (multiple gated transistor, or MGTR), combined with some additional circuit techniques are reported. In MGTR circuitry, linearity is improved by using transconductance linearization which can be achieved by canceling the negative peak value of g_m" of the main transistor with the positive one in the auxiliary transistor having a different size and gate drive combined in parallel. This enhancement, however, is limited by the distortion originated from the combined influence of g_m' and harmonic feedback, which can greatly be reduced by the cascoding MGTR output for the amplifier and by the tuned load for the mixer. Experimental results designed using the above techniques show IIP_3 improvements at given power consumption by as much as 10 dB for CMOS low-noise amplifier at 900 MHz and 7 dB for Gilbert cell mixer at 2.4 GHz without sacrificing other features such as gain and noise figure.

B. Bulk-Bias Control

This technique presents a g_m"-cancellation range extension method with bulk-bias control that was applied to a Multiple Gated Transistors (MGTR) technique, which is a linearity enhancement technique for RF amplifiers. Instead of adjusting the gate-biasing voltage of the auxiliary transistor (AT) (V_{shift}) in conventional g_m" -cancellation, we propose to use the bulk-biasing voltage, V_{BS}, which allows for range extension of the g_m"-cancellation of AT. The proposed technique does not require any other additional biasing circuits and has the benefit of consuming less power.

C. Gain-Enhancement Techniques

In this paper, gain-enhancement techniques suitable for folded cascode low-noise amplifiers (LNAs) at low-voltage operations are presented. By employing a forward bias and a capacitive divider at the body of the MOSFETs, the LNA circuit can operate at a reduced supply voltage while maintaining an enhanced gain due to suppression of the negative impact of the body transconductance. In addition, G_m-boosting stage is introduced to further increase the LNA gain at the cost of circuit linearity. Using a standard 0.18-mum CMOS process, two folded cascode LNAs are demonstrated at the 5-GHz band based on the proposed topologies.

D. Resistive Shunt -feedback

Extremely compact resistive-feedback CMOS low-noise amplifiers (LNAs) are presented as a cost-effective alternative to multiple narrowband LNAs using high-*Q* inductors for multiband wireless applications. Limited linearity and high power consumption of the inductorless resistive-feedback LNAs are analyzed and circuit techniques are proposed to solve these issues. A 12-mW resistive-feedback LNA, based on current-reuse transconductance boosting is presented with a gain of 21 dB and a noise figure (NF) of 2.6 dB at 5 GHz. The LNA achieves an output third-order intercept point (IP3) of 12.3 dBm at 5 GHz by reducing loop-gain rolloff and by improving linearity of individual stages. The active die area of the LNA is only 0.012 mm^2. A 9.2-mW tuned resistive-feedback LNA utilizing a single compact low-*Q* on-chip inductor is presented, showing an improved tradeoff between performance, power consumption, and die area.

E. Resistive-Feedback for Multiband Applications

A 3.1-10.6 GHz ultra-wideband low-noise amplifier (UWB LNA) with excellent phase linearity property (group-delay variation is only plusmn 16.7 ps across the whole band) using standard 0.13 mum CMOS technology is reported. To achieve high and flat gain and small group-delay variation at the same time, the inductive peaking technique is adopted in the output stage for bandwidth enhancement.

F. GBW and Linearity Enhancing Techniques

A CMOS distributed amplifier (DA) with distributed active input balun is presented that achieves a gain-bandwidth product of 818 GHz, while improving linearity. Each *gm* cell within the DA employs dual-output two-stage topology that improves gain and linearity without adversely affecting bandwidth (BW) and power. Comprehensive analysis and simulations are carried out to investigate gain, BW, linearity, noise, and stability of the proposed *gm* cell, and compare them with conventional *gm* cells.

G. Body Biasing in Multistage CMOS Low-Noise Amplifiers

Low-noise amplifiers (LNAs) are one of the important building blocks of wireless receivers. LNA design parameters such as gain, noise figure, linearity, input matching, and stability are important metrics and typically affect the overall performance of the receiver. The strong trade-offs among these design parameters often necessitate several design iterations. While many of these trade-offs are due to the nature of the circuit and are inevitable, it is desirable to decouple the effects of each parameter on the others. In this work, body biasing is introduced as a technique to enhance the linearity, to improve the noise figure and to provide gain variation. These techniques are presented in the context of a three-stage LNA. By applying body biasing in each stage, noise figure, gain variation and linearity of the overall amplifier are adjusted almost independently, i.e., with minimal interrelation among these design parameters. As a proof-of-concept, a prototype 4.4-GHz LNA is designed and fabricated in a 0.13- μm CMOS technology. The LNA achieves a minimum noise figure of 3.8 dB, maximum gain of 20.2 dB, and a maximum IIP3 of -14 dBm while consuming 3.6 mW from a 1.2 V supply.

H. Leakage Suppression

A low-noise multi-band transmitter for GSM quad-band and WCDMA is presented. Programmable parameters of the analog baseband and the RF frontend enable adaption for different protocols and frequency bands. A three-step carrier leakage calibration algorithm is proposed to suppress the leakage to -65 dBm at highest RF gain. Novel linearization methods are used in the low-pass filter and the driver power amplifier to meet the demand of 3G systems.

I. Multiband Feedback and Gain-Reuse

Receiver down-converter topologies are presented that provide simultaneous frequency conversion and baseband amplification within a mixer, in order to reduce power dissipation for a given dynamic range. The down-converted IF output of a mixer is reapplied to its input stage in a recursive manner, which significantly enhances the conversion gain, with current requirement determined primarily by the input transconductor of the mixer. Two down-converter topologies based on this technique are presented. One topology utilizes common-source NMOS devices as the RF input stage of the mixer, and reuses their transconductance for providing baseband gain. The second topology utilizes differential pairs as the RF input stage, and employs the transconductance of the tail current-source devices for baseband gain. Noise and linearity performance of the down-converters is analyzed, and the potential for enhancement of IIP3 through cancellation of nonlinear products is discussed.

J. Active Mixer Exploiting Noise Cancellation

A wideband CMOS active mixer is proposed with improved noise and linearity, merging a resistive feedback noise-canceling low-noise amplifier as its transconductor. The noise-canceling characteristic enables the transconductor with low noise over a wide frequency range. An auxiliary pMOS transistor is employed to cancel the third-order nonlinear currents of a composite transistor in the transconductor, and impair the second-order nonlinear currents of that. To enhance input equivalent transconductance, a bulk cross-coupled feedback is applied to the transistor in the transconductor with

large power consumption. Together with a current bleeding technique, comparable gain, noise, and improved linearity are achieved, but by reduced bias currents of the mixer.

III. CONCLUSION

Versatile low noise low power amplifier demanded and needed for recent technology like GSM, Wi-Max, WLAN, Satellite Communication, Mobile communication etc. in the review of Low noise amplifier, For improvement of the performance and linearity of low noise amplifier many number of techniques used in past decades are discuss like Adopting Multiple Gated Transistors Technique,Bulk-Bias Control,Gain-Enhancement Techniques

Capacitive-feedback, Resistive-Feedback, GBW and Linearity Enhancing ,Body Biasing in Multistage CMOS Low-Noise Amplifier, Leakage Suppression, Reuse, Active and inductively degenerated this all techniques discuss in detail and gives idea about the technology how to used to improve linearity of amplifier, Discuss techniques to improve noise figure, reduce power consumption, gives good impedance matching in input and output section of amplifier, discuss about the gain boosting technique, inductive peaking is a best technique to improve the gain of amplifier, all techniques used to improve of performance and characteristics of amplifier , noise rejection capability and impedance bandwidth over single band, dual band, multi-band and broad band, but recent technology demand and needed low noise amplifier with versatile future so that more discussion and research required in field of low noise amplifier. Compare and discuss recent techniques in table-1, reviewed low noise amplifier from origin and discuss development and find Different technologies are used for implementing the different designs in the different aspects

Table 1 Review of Techniques

Technique Used	Power Consumption	S-Parameter	Noise Figure
Adopting Multiple Gated Transistors	20mW	= -10	4dB
Bulk-Bias Control	10mW	= -8	4.5dB
Gain-Enhancement Techniques	5µW	= -12	3dB
Capacitive-feedback	20mW	= -7	5dB
Resistive-Feedback for Multiband Applications	20mW	= -11	4.7dB
GBW and Linearity Enhancing Techniques	50µW	= -12	3dB
Body Biasing in Multistage CMOS Low-Noise Amplifiers	10µW	= -13	2dB
Leakage Suppression	100µW	= -12	2dB
Multiband Feedback and Gain-Reuse	50µW	= -10	2.5dB
Active Mixer Exploiting Noise Cancellation	3mW	= -7	3.8dB

REFERENCES

[1] Tae Wook Kim; Bonkee Kim; Kwyro Lee" Highly linear receiver front-end adopting MOSFET transconductance linearization by multiple gated transistors"IEEE Journal of Solid-State CircuitsYear: 2004, Volume: 39, Issue: 1Pages: 223 - 229
[2] T. H. Jin; T. W. Kim"A 6.75 mW 12.45 dBm IIP3 1.76 dB NF 0.9 GHz CMOS LNA Employing Multiple Gated Transistors With Bulk-Bias Control"IEEE Microwave and
[3] Wireless Components LettersYear: 2011, Volume: 21, Issue: 11Pages: 616 - 618,
[4] H. H. Hsieh; J. H. Wang; L. H. Lu ",Gain-Enhancement Techniques for CMOS Folded cascode LNAs at Low-Voltage Operations"IEEE Transactions on Microwave Theory and Techniques Year: 2008, Volume: 56, Issue: 8 Pages: 1807 - 1816
[5] H. Y. Yang; Y. S. Lin; C. C. Chen"2.5 dB NF 3.1-10.6 GHz CMOS UWB LNA with small group-delay variation " IEEE Electronics Letters Year: 2008, Volume: 44, Issue: 8 Pages: 528 - 529,
[6] B. G. Perumana; J. H. C. Zhan; S. S. Taylor; B. R. Carlton; J. Laskar "Resistive-Feedback CMOS Low-Noise Amplifiers for Multiband Applications" IEEE Transactions on Microwave Theory and Techniques
[7] Year: 2008, Volume: 56, Issue: 5Pages: 1218 – 1225.
[8] P. Heydari, "A CMOS Distributed Amplifier With Distributed Active Input Balun Using GBW and Linearity Enhancing Techniques" IEEE Transactions on Microwave Theory and Techniques Year: 2012, Volume: 60, Issue: 5 Pages: 1331 - 1341,
[9] H. Rashtian; S. Mirabbasi" Aplications of Body Biasing in Multistage CMOS Low-Noise Amplifiers" IEEE Transactions on Circuits and Systems Year: 2014, Volume: 61, Issue: 6 Pages: 1638 - 1647,
[10] Y. Li; K. Han; C. Dong; C. Zhang; Y. Yu; X. Tan; N. Yan; Q. Chen; H. Min" A Multi-Band Low-Noise Transmitter With Digital Carrier Leakage Suppression and Linearity Enhancement" IEEE Transactions on Circuits and Systems Year: 2013, Volume: 60, Issue: 5Pages: 1209 - 1219,
[11] Han; R. Gharpurey" Recursive Receiver Down-Converters With Multiband Feedback and Gain-Reuse"IEEE Journal of Solid-State CircuitsYear: 2008, Volume: 43, Issue: 5Pages: 1119 – 1131.
[12] P. Asbeck, L. Larson, D. Kimball, and J. Buckwalter, "CMOS handset power amplifiers: Direction for the future," in Proc. IEEE Custom Integr.Circuit Conf., Sep. 2012, pp. 1–6.
[13] W. C. E. Neo, Y. Lin, X.-D. Liu, L. C. N. de Vreede, L. E. Larson, M.Spirito, M. J. Pelk, K. Buisman, A. Akhnoukh, A. de Graauw, and L.K. Nanver, "Adaptive multi-band multi-mode power amplifier using integrated varactor-based tunable matching networks," IEEE J. Solid-State Circuits, vol. 41, no. 9, pp. 2166–2176, Sep. 2006.
[14] J.Moon, J. Son, J. Lee, and B. Kim, "Amultimode/multiband envelope tracking transmitter with broadband saturated amplifier," IEEE Trans.Microw. Theory Techn., vol. 59, no. 12, pp. 3463–3473, Dec. 2011.
[15] Y. Cho, D. Kang, J. Kim, D. Kim, B. Park, and B. Kim, "A dual powermode multi-band power amplifier with envelope tracking for handset applications," IEEE Trans. Microw. Theory Techn., vol. 61, no. 4, pp.1608–1619, Apr. 2013.
[16] D. Kang, D. Kim, J. Choi, J. Kim, Y. Cho, and B. Kim, "A multimode/multiband power amplifier with a boosted supply modulator," IEEE Trans. Microw. Theory Techn., vol. 58, no. 10, pp. 2598–2608, Oct.2010.
[17] S. Yoon, I. Lee, M. Urteaga,M. Kim, and S. Jeon, "A fully-integrated 40–222 GHz InP HBT distributed amplifier," IEEE Microw. Wireless Compon. Lett., vol. 24, no. 7, pp. 460–462, Jul. 2014.
[18] H.-Y. Chang, Y.-C. Liu, S.-H. Weng, C.-H. Lin, Y.-L. Yeh, and Y.-C.Wang, "Design and analysis of a DC–43.5-GHz fully integrated distributed amplifier using GaAs HEMT-HBT cascode gain stage," IEEE Trans. Microw. Theory Techn., vol. 59, no. 2, pp. 443–455, Feb. 2011.
[19] P. Dennler, R. Quay, P. Brückner, M. Schlechtweg, and O. Ambacher,"Watt-level non-uniform distributed 6–37 GHz power amplifierMMIC with dual-gate driver stage in GaN technology," in IEEE Power Amplifiers Wireless Radio Appl., Jan. 2014, pp. 37–39.
[20] M. Chang and G.M. Rebeiz, "A 26 to 40 GHz wideband SiGe balanced power amplifier IC," in IEEE Radio Freq. Integr. Circuits Symp., Jun.2007, pp. 729–732.
[21] SiGe PA module for multi-band and multi-mode cellular-phone applications," in Proc. IEEE Int. Solid-State Circuits Conf., Feb. 2008,pp. 572–637.
[22] N. Demirel, E.Kerhervé, R. Plana,D. Pache, and D. Belot, "59–71GHz wideband MMIC balanced power amplifier in a 0.13 m SiGe technology," in Proc. Eur. Microw. Conf., Sep.–Oct. 2009, pp. 1852–1855.
[23] H. Zhang, H. Gao, and G.-P. Li, "Broad-band power amplifier with a novel tunable output matching network," IEEE Trans. Microw. Theory Techn., vol. 53, no. 11, pp. 3606–3614, Nov. 2005.
[24] S. Kang, U. Kim, Y. Kwon, and J. Kim, "A multi-mode multi-band reconfigurable power amplifier for low band GSM/UMTS handset applications,"in IEEE Power AmplifiersWireless Radio Appl., Jan. 2013,pp. 16–18.
[25] F. Aref and R. Negra, "A fully integrated adaptive multiband multimode switching-mode CMOS power amplifier," IEEE Trans. Microw.Theory Techn., vol. 60, no. 8, pp. 2549–2561, Aug. 2012.

[26] U. Kim, S. Kang, J.Woo, Y. Kwon, and J. Kim, "A multiband reconfigurable power amplifier for UMTS handset applications," IEEE Trans.Microw. Theory Techn., vol. 60, no. 8, pp. 2532–2542, Aug. 2012.
[27] Hur, O. Lee, C.-H. Lee, K. Lim, and J. Laskar, "A multi-level and multi-band class-D CMOS power amplifier for the LINC system in the cognitive radio application," IEEE Microw. Wireless Compon. Lett.,vol. 20, no. 6, pp. 352–354, Jun. 2010.
[28] G. Lee, J. Lee, and J.-I. Song, "A single chipmultiband power amplifier using active load modulation techniques," in IEEEMTT-S Int. Microw.Symp. Dig., Jun. 2012, pp. 1–3.
[29] D. Qiao, R.Molfino, S. M. Lardizabal, B. Pillans, P. M. Asbeck, and G.Jerinic, "An intelligently controlled RF power amplifier with a reconfigurable MEMS-varactor tuner," IEEE Trans. Microw. Theory Techn.,vol. 53, no. 3, pp. 1089–1095, Mar. 2005.
[30] J. Kim, Y. Yoon, H. Kim, K. H. An,W. Kim, H.-W. Kim, C.-H. Lee,andK. T.Kornegay, "Alinear multi-modeCMOS power amplifier with discrete resizing and concurrent power combining structure," IEEE J.Solid-State Circuits, vol. 46, no. 5, pp. 1034–1048, May 2011.

