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Design of Asynchronous Viterbi Decoder using Dual-Rail Protocol for Low Power Consumption

Sonali V. Mothe [1], Prof. Surekha Tadse Kalambe [2]
[1] *Student, M.Tech (Communication Engineering) Electronics and Telecommunication Engineering G. H. Raisoni College of Engineering Nagpur, India.*
[2] *Research Scholar Electronics and Telecommunication Engineering G. H. Raisoni College of Engineering Nagpur, India.*

Abstract—The main objective of this paper is to design Asynchronous Viterbi Decoder system. To design asynchronous Viterbi decoder, there is need to design a convolution encoder, this work defines the design of Convolution Encoder for constraint length K= 3 and code rate r= 1/3 and input bit k=1. As the literature review shows that the input bit sequence is four times of the constraint length of the encoder. The constraint length of encoder is K=3, then the input is provide to encoder is 12 bit long i.e. four times of constraint length. To make the system asynchronous, there is a need of local handshaking protocol. Here dual-rail protocol is used to make the system asynchronous from synchronous. As Viterbi decoder is widely used in portable devices, so the important thing is to reduce the consumption of power from the device for better reliability. Therefore the focus of this research is to lower the power consumption, for that the system needs to make asynchronous, by applying the handshake protocol as Dual-Rail Protocol. So the main aim of this paper is to design of asynchronous viterbi decoder using dual rail protocol for low power consumption
Keywords— Viterbi Algorithm, VHDL, Encoder, Asynchronous System, Handshake Protocol (Dual Rail Protocol), Power Consumption, Soft Decoding.

I. INTRODUCTION

The increasing need of wireless communication devices, there is need to demand for severe precedent on speed and power consumption of wireless devices. Viterbi decoder plays an important role in communication devices for correcting the errors from the communication applications and it is used in wireless applications. Therefore, to decline the consumption of power from the Viterbi Decoder, it becomes a main objective in designing of the system. The design of asynchronous system has highly relieved from the problems of synchronous clocking system. This paper deals with the problem of power consumption and proposed a new asynchronous technique i.e. by applying a Dual rail protocol to consume less power. This proposed design has an advantage of low power, self-adaptive startup and delay insensitive which able to fulfill the requirement of low-power consumption in portable device. Asynchronous means self-timed system i.e. the working manner of asynchronous design is clock less. The difficulties can be avoided which comes from the clocking system. As far as the power consumption is concerned, synchronous design consist of more switching action than the asynchronous design. As large as the switching action, the more power will be gained by the system. Oppositely, in asynchronous design parts consume slight power and switching action is co-relate with the work done which is use full an important factor for battery regulated systems. Lesser the clocking system, lower the consumption of power. Asynchronous design outcomes low electromagnetic radiation than the synchronous design. Asynchronous design or Synchronous design can be treated in the operation of the Viterbi decoder. Dual-rail protocol algorithm is a common asynchronous technique which is used to implement an asynchronous data

path. There are two types of decoding techniques i.e. Hard Decoding & Soft decoding which is used to decode the viterbi decoder. Viterbi decoders are from those devices which consumes large power. In this paper soft decoding is used to make decoder, as soft decoding is much reliable than the hard decoding. Here the asynchronous Viterbi Decoder is made with the use of soft decoding technique.

II. ENCODER

In this paper, the encoder consists of two flip flops, one input & three outputs. Encoder code rate is 1/3. The constraint length K of encoder is 3. The output format of encoder is as shown below:-

Out0 = I/P XOR FF0
Out1 = I/p XOR FF1 XOR FF0
The input &output sequence is
Input Sequence: 011010111100.
OutputSequence: 000,111,100,100,000,011,000.100,011,011,100,111.
The output of encoder is a part of current input & current state. It consists of multiple ex-or gates and more than one shift register.

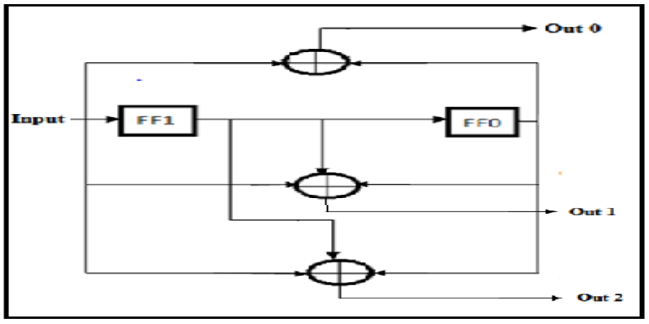

Fig.1 shows the 1/3 Convolution Encoder

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III. VITERBI DECODER

Viterbi decoder block diagram consist of four blocks as explained below:-

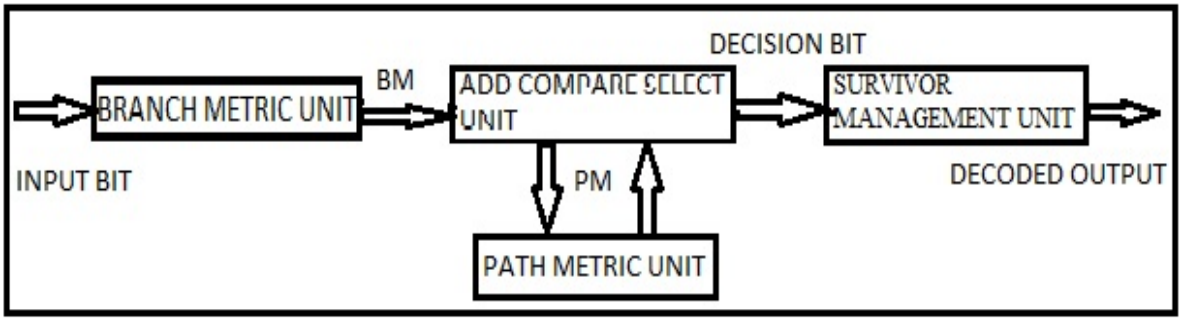


Fig2. Shows the block diagram of viterbi decoder

1) BRANCH METRIC UNIT: - BMU calculates the branch metric from the received sequence bit, this calculated branch metrics are then fed to the ACSU block.
2) ADD COMPARE SELECT UNIT: - As the name suggest the function of ACSU is to add & compare the branch metric and the path metric as shown in block diagram. ACSU selects the minimum metric or path as decision bit and this decision bit of each state provided to the further block i.e. PMU.
3) PATH METRIC UNIT: - The metric of current state path is stored in a PMU.

4) SURVIVOR MANAGEMENT UNIT: - SMU stores decision bit and it regained from the SMU. SMU decodes the source sequence bits and then forward the survivor path.

Moreover, as the value of constraint length k increases, the consumption of power and complexity of the system also increases accordingly. There are some limitations of Viterbi algorithm, code rate and data rate has the large variation. It is necessary to design the algorithm of Viterbi decoder to reduce the consumption of power for low data rate.

The Viterbi algorithm can be divided into parts:-

- Calculates the metrics of the branch of the trellis.
- Then this metrics can be compared of each state by soft decoding technique i.e. 0 indicates +3 and 1 indicates -3
- By comparing this soft decoding metrics and selects minimum metric from each state.
- By following step 3 up to 12 stages, and finds the shortest path from the each transition state. The shortest path is known as survivor path.

IV. SOFT DECODING TECHNIQUE

In this paper soft decoding is used to decode the Viterbi decoder. Soft decoding is used to calculate Euclidean distance of the each branch of each state. In this design the soft decoding technique is fixed in the form of 3 & -3. Zero indicates through +3 & one indicates through -3. If the metric of any state is in negative form then 2's complement of that negative value is taken for further procedure. Likewise, all branch metrics are calculated, and minimum path is taken as survivor path for the trellis. On the other hand hard decoding does not need to define their metrics as +3 or -3. It is just define by 0 or 1 only. Hard decoding is used to calculate the hamming distance between the respective metrics. In soft decoding it's not necessary to fixed 0 as +3 or 1 as -3, it can oppositely fixes as per the convenience. There is important to remember that +3 & -3 are used for only 3 bits metric i.e. from 0 to 7. If the no. of bits increases i.e. from 0 to 15, then the soft decoding values are also increase like +5 & -5.

For example: - This table shows the possible value of Branch metrics, Outputs of Encoder i0, i1&i2 and Path Metric

BMU 000	+3+3+3	+9
BMU 111	-3-3-3	-9
BMU 001	+3+3-3	+3
BMU 011	+3-3-3	-3
BMU 110	+3+3-3	+3
BMU 101	-3+3-3	-3
BMU 010	+3-3+3	+3
BMU 100	-3+3+3	+3

V. SYNCHRONOUS SYSTEM VERSUS ASYNCHRONOUS SYSTEM

There are various ways to transfer serial data protocols. Two types of Protocols are used to transfer serial data which are synchronous & asynchronous:

In synchronous system, special clock signal is needed through which the synchronous data can be access by the sender & receiver by the equal clock. The master permits to maintain a clock signal for all receivers to transfer the data.

In asynchronous system, no need to require special clock signal for the sender and receiver. To transfer the serial data, sender & receiver needs to agree. The internal circuits of sender & receiver both needs to setup internal circuits for the agreement to transfer of serial data. The fig. shows comparison of synchronous Vs asynchronous.

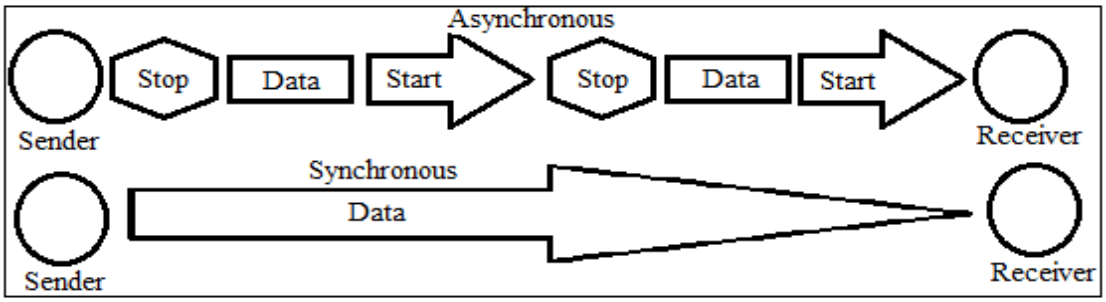


Fig3. Shows the comparison of asynchronous & synchronous system

VI. ASYNCHRONOUS DUAL-RAIL PROTOCOL

Asynchronous system consists of some blocks which communicate with each other via handshaking protocol. Asynchronous channel comprises bundle of protocols to share its information data within the system blocks. There are two types of transmission protocol which are:

1) When the protocol consists of one wire to transmit per bit of data, when data bit sequence is authenticated is known as single rail/bundle data protocol.
2) Alternatively, When the protocol consists of two wire to transmit per bit of data, when the data bit sequence is authenticates is known as dual-rail protocol. In this paper, dual-rail protocol is used to asynchronous the system design.
There are two types of dual-rail protocol, 4 Phase & 2 phase dual rail protocol. Dual rail means two rails that mean two rail or wires. These wires show the empty data or valid data. Dual Rail protocol is delay insensitive protocol; it is very robust in terms of delay.
4 phase dual Rail protocol is most commonly used for asynchronous the system. The main objective of this paper is to lower the consumption of power; dual rail algorithm is used for lower the consumption of power. There are some basic steps, through which the algorithm can be design, 2 phase dual rail algorithm & 4 phase dual rail algorithm are simpler in designing.

VII. SIMULATION RESULT

The following windows define the simulations of Convolution Encoder, Asynchronous Viterbi Decoder using Model SimSE6.3f from VHDL codes & Power is analyzed in Xilinx ISE13.2.

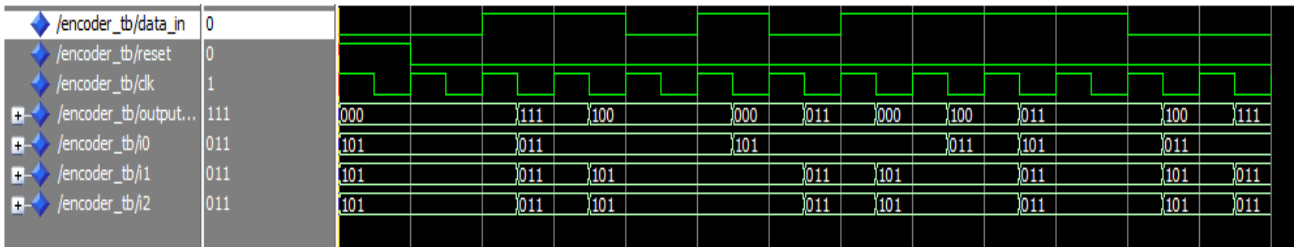


Fig. 4 shows the 1/3 convolution encoder

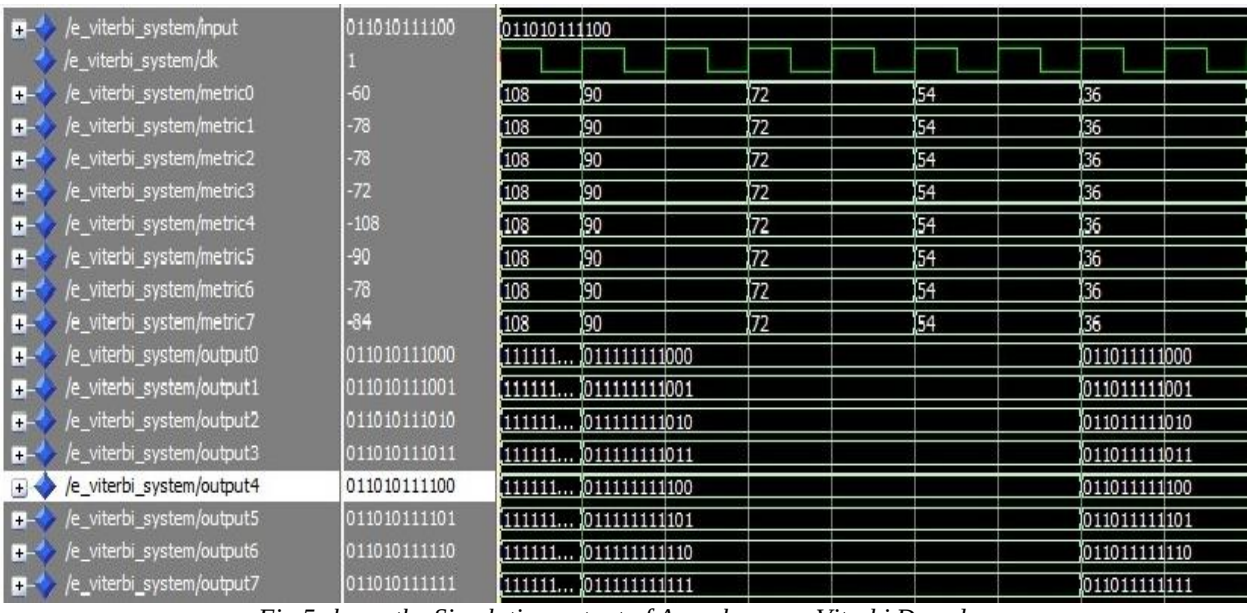
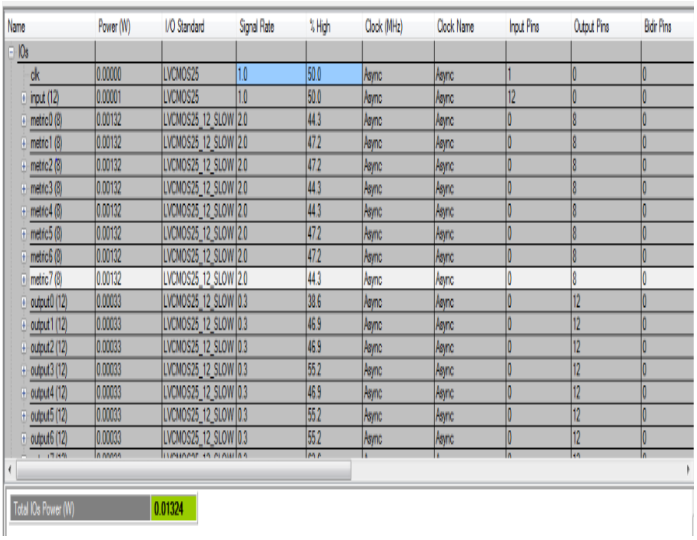


Fig 5 shows the Simulation output of Asynchronous Viterbi Decoder

Feature	Result
Design	Asynchronous Viterbi Decoder
Protocol Used	Dual-Rail Protocol
No. of states (K)	3
Code Rate (r)	1/3
Input Bit (k)	1
Frequency (F)	10MHz
Power Consumption(mW)	13.24mW

Fig. 6 shows the power Analysis



Name	Power (W)	I/O Standard	Signal Rate	% High	Clock (MHz)	Clock Name	Input Pins	Output Pins	Bidir Pins
IOs									
clk	0.00000	LVCMOS25	1.0	50.0	Async	Async	1	0	0
input (12)	0.00001	LVCMOS25	1.0	50.0	Async	Async	12	0	0
metric0 (8)	0.00132	LVCMOS25_12_SLOW	2.0	44.3	Async	Async	0	8	0
metric1 (8)	0.00132	LVCMOS25_12_SLOW	2.0	47.2	Async	Async	0	8	0
metric2 (8)	0.00132	LVCMOS25_12_SLOW	2.0	47.2	Async	Async	0	8	0
metric3 (8)	0.00132	LVCMOS25_12_SLOW	2.0	44.3	Async	Async	0	8	0
metric4 (8)	0.00132	LVCMOS25_12_SLOW	2.0	44.3	Async	Async	0	8	0
metric5 (8)	0.00132	LVCMOS25_12_SLOW	2.0	47.2	Async	Async	0	8	0
metric6 (8)	0.00132	LVCMOS25_12_SLOW	2.0	47.2	Async	Async	0	8	0
metric7 (8)	0.00132	LVCMOS25_12_SLOW	2.0	44.3	Async	Async	0	8	0
output0 (12)	0.00033	LVCMOS25_12_SLOW	0.3	38.6	Async	Async	0	12	0
output1 (12)	0.00033	LVCMOS25_12_SLOW	0.3	46.9	Async	Async	0	12	0
output2 (12)	0.00033	LVCMOS25_12_SLOW	0.3	46.9	Async	Async	0	12	0
output3 (12)	0.00033	LVCMOS25_12_SLOW	0.3	55.2	Async	Async	0	12	0
output4 (12)	0.00033	LVCMOS25_12_SLOW	0.3	46.9	Async	Async	0	12	0
output5 (12)	0.00033	LVCMOS25_12_SLOW	0.3	55.2	Async	Async	0	12	0
output6 (12)	0.00033	LVCMOS25_12_SLOW	0.3	55.2	Async	Async	0	12	0
Total IOs Power (W)	0.01324								

Fig. 7 shows the Total Power

Logic Utilization	Used	Available	Utilization
Name of Slices	649	5888	11%
Name of Slices Flip flops	61	11776	0%
No. of 4 Input LUTs	1324	11776	11%
No. of Bonded IOBs	173	372	46%

Fig. 8 Shows the Device Utilization summary

Fig. 9 shows the RTL schematic

VII. CONCLUSION

The implemented design of Asynchronous Viterbi Decoder is for code rate r = 1/3, constraint length K= 3 and input bit k=1. Asynchronous Viterbi Decoder reduces the consumption of power. Dual Rail protocol is used to Asynchronous the system. Through which the consumption of power is achieved 13.24 mW for the frequency 10MHz. This design of Asynchronous Viterbi decoder is Simulate in Model SimSE6.3f and Power is analyzed in Xilinx ISE13.2 successfully.

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