Scientific Journal Impact Factor (SJIF) : 1.711
International Journal of Modern Trends in Engineering and Research
ISSN (ONLINE) : 2349 - 9745 ISSN (PRINT) : 2393 - 8161

An Overview of Micro-Architecture Design for the 32-bit VLIW DSP

A.S.Korde[1], Prof. S. R. kale[2]

[1,2] *E & TC department, SVIT Chincholi, Nashik*

Abstract—Now a days there are different applications such as image processing, speech recognition, medical imaging, oil prospecting, etc, in which DSP take essential part [1], [2]. But some applications cannot give the high performance using general purpose processors so due to this some specific digital signal processing algorithms including Fourier transform, digital filtering, etc are as great solution which is strong optimizations of their architectures for increasing the performance of those applications, hence, the emergence of digital signal processors (DSPs) can be considered. In this paper we proposed the overview of the micro-architecture design of 32-bit VLIW DSP based on the top level architecture.

Keywords—Digital Signal processor, Micro-architecture, VLIW

I. INTRODUCTION

In real life such as communications, medical imaging, radar & sonar, high fidelity music reproduction, oil prospecting, etc, digital signal processing is increasingly important for applications. In an efficient manner will help the system be more attractive, as applications become more complex, the processing of digital signals. An architecture optimized for operational needs of digital signal, a digital signal processor is a specialized microprocessor. Although DSP processors have a comprehensive change in the past few decades, there are still common features in most DSP processors today such as multiple memory banks with independent buses, specialized instruction sets, addressing modes, control and peripherals.

Modern DSP architectures [5] can be divided into 3 or 4 categories. To encode a single operation, multi-issue processors use very simple instructions that typically. By issuing and executing instructions in parallel groups rather than one at a time, these processors achieve a high level of parallelism. Allowing multi-issue processors to execute at higher clock rates than conventional or enhanced conventional DSP processors, using simple instructions simplifies instruction decoding and execution. Multiple instructions in parallel are VLIW and superscalar, the two sub-categories of implementation of this architecture that execute. The biggest difference between them is how instructions are grouped for parallel execution. To include a 40-bit adder and a logical operation unit, ALU was constructed with CISC based processor [6]. Output data from ALU are optionally shifted by barrel shifter. The implementation is not flexible enough for byte-operations, although all of word-arithmetic and logical operations can be carried out by this design. For the 16-bit DSP processor, introduced a RISC-based architecture [7]. ALU is responsible for arithmetic and logical operations, MAC calculations. In fact, the ALU is constructed to include three sub units: MAC, LOGIC and ARITH units. In term of parallel computation, this design is not effective. The ARITH unit is free and vice versa, for example, when the MAC unit is busy. It does not provide an effective method to compute on byte-data, although this ALU has a benefit of low complexity since only simple operations are supported.

II. LITERATURE SURVEY

Generally there are different processors are used for multiprocessor architecture such as VLIW architectures, superscalar architectures, or SIMD architectures, depends on the application [9].

The **conventional DSP processor [3]** are the low cost, low performance which executes one instruction per clock cycle and use the complex, multi-operation type of instructions. Examples: Lucent DSP16xxx, ADI ADSP-2116x. Conventional DSP [11] executes one instruction per clock cycle, Complex, "compound" instructions encoding many operations, highly constrained, non-orthogonal architectures, dedicated hardware for loops and other execution control.

In **Enhanced conventional processor [3]** DSP architecture hardware improvement and these hardware enhancements are combined with an extended instruction set that takes advantage of the additional hardware by allowing more operations to be encoded in a single instruction and executed in parallel. So the problem that, they are difficult to program in assembly language and they are unfriendly compiler targets. Using conventional DSP processor [11] can increasingly complex, hard-to-program architectures, Poor compiler targets. The enhanced conventional DSP processor is the SIMD (Single Instruction Multiple Data), provides more parallelism with multi-operation data path. With SMID architectures having loss of generality, high program memory usage, often support only fixed point architectures.

The next is **Multi-issue architecture [3**] used to achieve the high performance .These architecture uses a high level of parallelism by issuing and executing instructions in parallel groups rather than one at a time. The VLIW multi-issue architecture with compile time instruction scheduling and typically four or more instructions per cycle with flexible instruction grouping and another multi-issue architecture with runtime instruction scheduling [11], Examples of VLIW: TI TMS320C6xxx, Infineon Carmel. VLIW architectures required less complexity hardware whereas superscalar hardware more complexity because logic to find instruction level parallelism in instruction code. Example of superscalar DSP: ZSP ZSP164xxProgrammable DSPs are pervasive in the wireless handset market for digital cellular telephony. Author[1] present the argument that DSPs will continue to play a dominant, and in fact increasing, role in wireless communications devices by looking at the history of DSP use in digital telephony, examining the DSP-based solution options for today's standards, and looking at future trends in low-power DSPs.

This paper [4] presents a new method for reproduction of music in multichannel audio systems. The proposed method separates signals from individual channels into their direct and diffuse components which are then sent to different speaker elements. The direct components are sent directly to the listener, while the diffuse components are additionally scattered. The purpose of this scattering of diffuse components is twofold: first, it eliminates spurious localization cues which may be created by reproducing the sound using a small number of speakers (three to five), and second, it provides additional diffusion which improves the envelopment experience. We investigate two methods to separate direct and diffuse sound field components, both of which assume the knowledge of the impulse response of the performance auditorium to the corresponding microphones. One method is based on techniques for multichannel equalization, while the other uses techniques for signal reconstruction after oversampled filter-bank processing. The latter method turns out to be computationally more manageable. In listening tests, subjects preferred music reproduction which separates direct and diffuse sound fields to reproduction in which both sound fields are sent to the same speaker elements.

III. OVERVIEW OF VLSI DSP ARCHITECTURE

The general architecture of DSP SoC [8] consists of DSP core, peripheral controller, external memory controller, power management as well as acceleration hardware such as FFT core, DCT core, DMA units (Direct Memory Access) as shown in fig. 1.

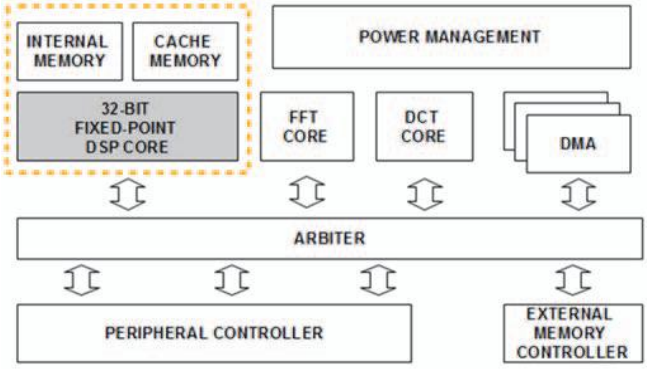

Figure 1 General Architecture of DSP SoC

From this architecture we consider the 32-bit DSP core which consists of Instruction Fetch unit, Instruction Decode unit, and four executional units, 32 32-bit general-purpose registers, control registers, interrupt controller and instruction cache as in Figure 2.

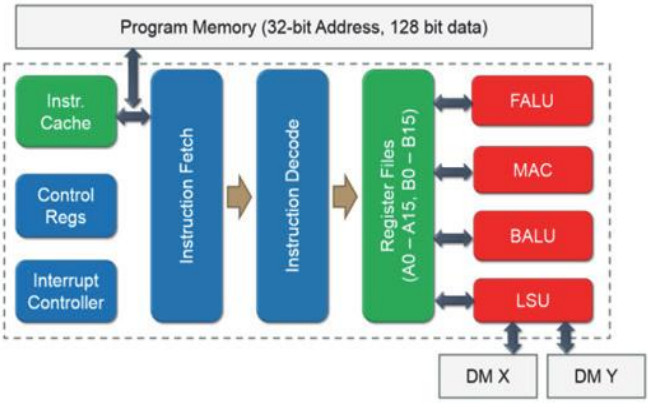

Figure 2 Top Level Architecture of DSP core

VLIW architectures typically use simple, RISC-based instructions. More orthogonal than the complex, compound instructions traditionally used in DSP processors. Instruction parallelism is exploited to speed up the high-performance microprocessors.

Compared to the dynamically hardware-scheduled superscalar processors, VLIW machines have low-cost compiler scheduling with deterministic execution time and thus become the trends of high-performance DSP processors. But VLIW processors are notorious for their poor code density, because the unused instruction slots must be filled by NOP. The situation gets worse when the parallelism is limited. Variable-length VLIW eliminates NOP with alternative functional unit (FU) codes for run-time instruction dispatch and decoding, compared to the conventional position-coded VLIW processors (i.e. each FU has a corresponding bit-field in the instruction packet). Indirect VLIW has an addressable internal micro-instruction memory (i.e. the programmable VIM) for the instruction packets.[10]

IV. MICRO-ARCHITECTURE DESIGN

A processor is central component of computer but now a days the processor are embedded in many components such as game consoles, consumer electronic devices and cars.

Pipelined Micro-architecture:

Generally the micro-architecture [12] is pipelined in three different stages as instruction fetch, instruction decode & instruction Execution.

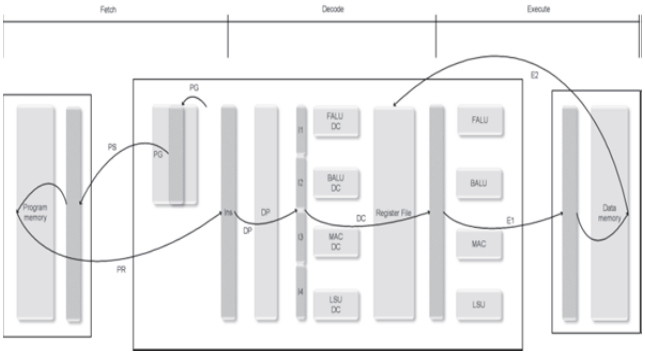

Figure 3 The pipeline micro architecture of 32-bit DSP

V. CONCLUSION AND FUTURE WORK

In this paper, we present an overview of micro-architecture design for the32-bit VLIW DSP. In this, we compared the performance and area cost of traditional and VLIW DSP architectures for compiled DSP applications. VLIW architectures can provide an improvement in performance compared to traditional architectures by executing multiple instructions/cycle. This is due to having more flexibility for parallelism and less restrictive.

In future work, by using the Verilog HDL and simulated in Altera ModelSim tool, this micro-architecture will be implement with application.

REFERENCES

[1] Gatherer A., Stetzler T., McMahan M., and Auslander E., "DSP-based Architectures for Mobile Communications: Past, Present, and Future", IEEE Communications Magazine, Vol. 38, Issue 1, pp. 84 – 90, Jan2000.

[2] Yagi M., Shibata T., "An Image Representation Algorithm Compatible with Neural-Associative-Processor-Based Hardware Recognition Systems", IEEE Trans. Neural Networks, Vol. 14, No. 5, pp. 1144 –1161, Sep. 2003.

[3] Jennifer Eyre and JeffBier **"**The Evolution of DSP Processors", 2000, Berkeley Design Technology Inc

[4] Olswang, B.S. ; LOUD Technol. Inc., Wodinville, WA ; Cvetkovic, Z.,"Separation of Audio Signals Into Direct and Diffuse Sound fields for Surround Sound", in Procs. of IEEE International Conference onAcoustics, Speech and Signal Processing, 2006.

[5] Edwin J. Tan and Wendi B. Heinzelman. "DSP architectures: past, present and futures. *SIGARCH Comput. Archit." News* 31, 3 (June 2003),pp. 6-19.

[6] Donghoon Lee, ChanwonRyu, Jusung Park, Kyunsoo Kwon and Wontae Choi, "Design and implementation of 16-bit fixed point digital signal processor", IEEE International SoC Design Conference (ISOCC), vol.2, pp. II-61 – II-64, 2008.

[7] Khoi-Nguyen Le-Huu, Thanh T. Vu, Diem N. Ho, Anh-Vu Dinh-Duc,"Towards a VLIW Architecture for the 32-bit Digital Signal Processor Core", in Procs. of the 5th FTRA Int. Conf. on Computer Science and its Applications (CSA) 2013.

[8] Khoi-Nguyen Le-Huu, Thanh T. Vu, Diem N. Ho, Anh-Vu Dinh-Duc, "Towards a RISC Instruction Set Architecture for the 32-bit VLIW DSP Processor Core", in Procs. of the IEEE Region 10 Technical Symposium (TENSYMP 2014), 2014.

[9] Khoi-Nguyen Le-Huu, Thanh T. Vu, Quoc-Minh Dang-Do, VyLuu, Trong-Tu Bui, Anh-Vu Dinh-Duc, "A Proposed RISC Instruction Set Architecture for the MAC Unit of 32-bit VLIW DSP Processor Core", in Procs. of the 2nd International Conference on Computing, Management and Telecommunications (ComManTel 2014), 2014.

[10] Tay-Jyi Lin, Chin-Chi Chang, Chen-Chia Lee, and Chein-Wei Jen, "An Efficient VLIW DSP Architecture for Baseband Processing", in Proceedings of the 21st International Conference on Computer Design (ICCD'03),IEEE 2003

[11] Evaluating the DSP Processor OptionsBerkeley Design Technology, Inc.www.BDTI.com

[12] Khoi-Nguyen Le-Huu, Anh-Vu Dinh-Duc, Tin T. Nguyen, "A Micro-Architecture Design for the 32-bit VLIW DSP Processor Core" APCC , IEEE 2014