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Synthesis and Implementation of PLC on FPGA

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Abstract- Programmable logic controller (PLCs) has become an indispensable control unit in the Industrial control field. But the performance of traditional PLC will be restricted by the length of ladder diagram and the operation speed of the microprocessor. It is difficult to adapt to the requirements of high-speed control in modern industry. Therefore, figuring out a way to realize high-speed control becomes more and more important. Field programmable gate array (FPGA) has characteristics of supporting high-speed parallel execution and hardware configuration. Realizing the function of PLC by it can greatly improve the execution speed of control logic and this is an important way to solve the current problems of PLC. The performance of programmable logic controllers is often constrained by the microprocessor and the real-time firmware of the controller. Field programmable gate arrays (FPGAs) are an attractive potential implementation medium for high-speed control because of their fast and parallel execution and programmable nature. Ladder Diagrams are a standard graphical programming method for industrial controllers, but compilers from Ladder Diagrams to FPGA hardware do not yet exist.

So this Project is the conversation of Ladder to VHDL programming in order to meet the FPGA advantages. The project is to implement Batch Processing Application on FPGA based PLC and to have a comparative study on results when implemented on it. The Batch Processing Application the contents are mixed in the user defined proportion taking into consideration of various parameters like the weight of the content used, time each hopper of the content will open in order to pour into the mixer hopper. Then at what temperature and pressure the content is mixed is to be maintained. The FPGA based PLC plays important role in opening and closing of the solenoid valve of each hopper, if the timing delay occurs then mixer is not mixed in the proper proportion. In order to do so the application is implemented on PLC and FPGA based PLC controlled, and the comparison is done related to it.PLC, based on FPGA, can greatly improve the speed of logic control.

Keywords- FPGA, Spartan 3, PLC

I. INTRODUCTION

Programmable logic controllers (PLCs) are a main stay for industrial process control and automation applications. They are low-cost, reliable, easy to use, and have been proven with years of successful operation. Their discrete analog and digital I/O features and ability to close control loops in the hundreds-of-hertz range meet many application needs. Unfortunately, not all applications easily fit into these constraints. Many new approaches to machine building have necessitated higher-performance controllers with innovative architectures. FPGA combines the real-time computing power of a computer with the reliability and flexibility of a field-programmable gate array (FPGA). The FPGA portion of the RIO architecture enables three core benefits over traditional control systems: high-performance parallel processing, custom hardware flexibility, and hardware logic

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II. LITERATURE SURVEY

Field Programmable Gate Array (FPGA) is quite popular today for its parallel execution mechanism and Reconfigurable hardware structure [1]. Programmable Logic Controller (PLC) is a user friendly, microprocessor based specialized computer that carries out control functions of many types and that of different levels of complexities [2]. The PLC will operate any system that has output devices that go on/off (known as discrete or digital outputs) or vary proportionately (known as analog outputs). The first PLC system evolved from conventional computers in the late 1960s and early 1970s. Though the late 1970s, improvements were made in the PLC programs to make them somewhat more user friendly. PLCs are also referred to as Programmable Controllers or Sequential Processors (i.e. devices that handle step by step execution of operations) that are widely used in commercial and industrial applications.

The CVT robot design, shown in fig. 3, will be mated to a new spherical CVT design currently in development.. The new there is metal-to-metal contact yielding a more controllable system with a compact design and a maximum sustainable input torque of 0.56 N-m; with a spherical CVT design.

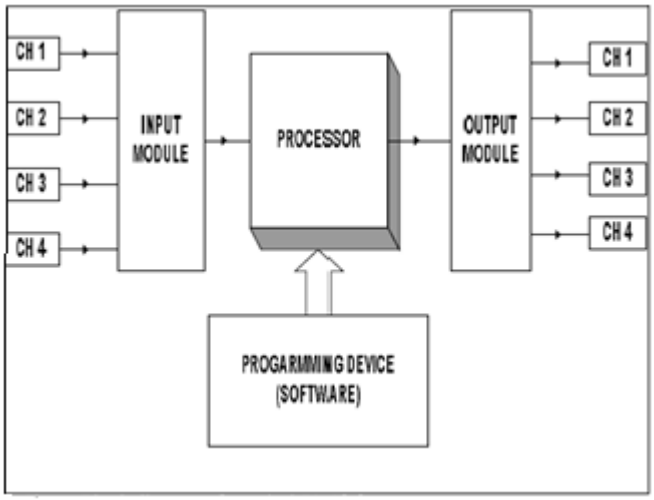


Figure 1. Block Diagram of Typical PLC

FPGA TECHNOLOGY:

Running advanced algorithms, such as field-oriented control (FOC) for brushless DC motors, can reduce power consumption and increase the life of components. These control algorithm advances are making machines more efficient, but often the algorithms need too much computational power to run on a PLC. For example, an FOC controller must continuously compute the vector control algorithm at a rate of 10 to 100 kHz. In parallel with the control algorithm, additional intellectual property (IP) blocks such as the high-speed PWM outputs need to execute without affecting the

timing of the control algorithm.. Moreover, with the reconfigurable nature of FPGAs, you can adjust the control algorithm whenever necessary.

A PLC designed using FPGA technology results in better solution providing following advantages:

(a) Short product development cycle

Due to the use of standard HDLs and runs directly in silicon, engineers can try out various types of implementation and hence, product development time is reduced significantly.

(b) Flexibility

Design engineers (PLC manufactures) can easily upgrade the Micro PLC designs. For example some feature or instructions could be added in the existing designs, simply by changing HDL and configuring the same FPGA chip for the modified designed of Micro PLC.

(c) Accuracy

This design provides parallel concurrent execution of blocks in hardware, hence provides better performance and accuracy as compared to conventional PLC.

(d) Very High Speed Performance

These design is based on FPGA that performs all tasks in parallel, hence execution of the proposed system design is very fast compare to conventional PLC as the later performs all the operations sequentially.

(e) Cost Effective and Compactness

Due to advantages mentioned above, designers can meet the market requirements by satisfying customer needs with improvement in the performance or functionality of the PLC product. These features result in high performance, low cost and compact designs as compared to the other available solutions.

III. PROPOSED METHOD AND RESULTS

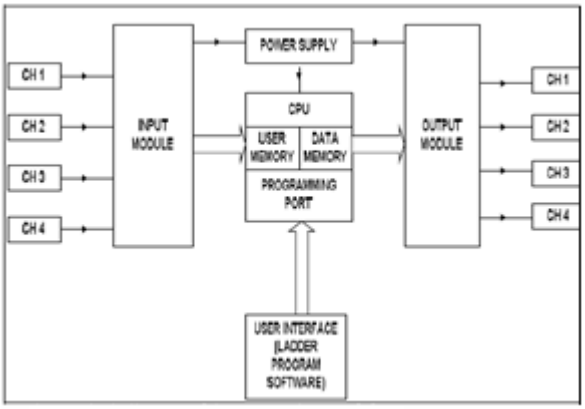


Figure 2. Block diagram of proposed system

A programmable logic controller, PLC or programmable controller is a digital computer used for automation of typically industrial electromechanical processes, such as control of machinery on factory assembly lines, amusement rides, or light fixtures. PLCs are used in many industries and machines.

Field Programmable Gate Arrays (FPGAs), offers an alternative solution for complex processing. They offer optimum performance, reduced power consumption, parallel processing, and the flexibility associated to hardware. This fact has leaded some PLC manufacturers to design a new class of PLC based on FPGAs instead of on sequential processors .The LD network is widely used method for describing control algorithms. This method has been inherited from relay control systems. Contacts and coils represent logic dependencies between signals and function blocks. The LD network processing speed can be increased by parallel execution of the logic operation in

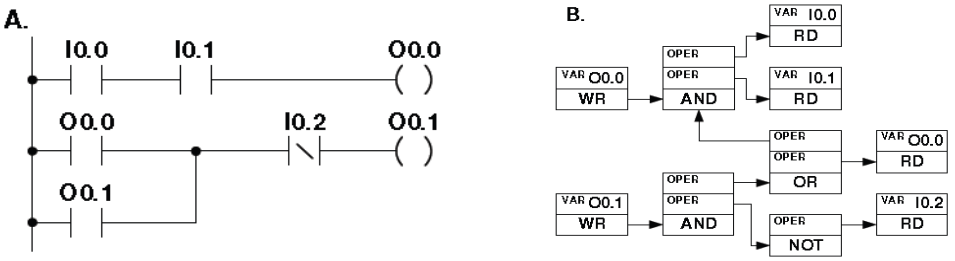
programmable hardware. Transforming logic dependencies into combinatorial logic allows increasing performance several orders of magnitude.
The majority of PLC manufacturers use the ladder logic diagram programming language to program their programmable logic controllers (PLCs). Some manufacturers prefer using logic gate circuits or Boolean expressions to program their PLCs.

Example: - The function of an XOR gate is simulated in the electric circuit displayed in below Figure. Notice that the lamp will be on if one switch is open while the other switch is closed. Figure below displays a ladder logic diagram that performs the function of an XOR gate. When I:0/0 is on, I:0/1 must be off and vice versa in order to turn on output O:0/0. When either Pushbutton #1 or Pushbutton #2 is pressed, the output is ON. When both pushbuttons are pressed, output is OFF.

Creating logic gate circuits from ladder diagrams

The first step in this process to find the Boolean expression that represents the ladder logic diagram. You can then draw the logic gate circuit using the Boolean expression.

Step two is writing the equivalent VHDL code



The Basic implementation is to give PLC and FPGA inputs at different frequency and check the corresponding outputs.

Simulation Results

For simulation only one output, four inputs and 17 select lines are used. The results shown in Fig. 9 are the results of main architecture of system inside FPGA.

IV. CONCLUSIONS

This paper is describes only concept of a new implementation approach to FPGA based PLC. This design is limited to only four digital inputs and outputs. To overcome the performance limitation of microprocessor based PLC; the suggested approach provides better result. The idea described here is best suitable for small-scale application where the need is limited number of instructions at reasonable cost, which also offer best performance, high speed and compact design approach.
For implementation of the suggested solution, some studies on implementation of control programs into logic description in form of Hardware Description Language (HDL) have been carried out. Hence, it becomes necessary f or t he user of proposed design to have knowledge of design tools to translate, integrate and implement the logic circuit in FPGA.

REFERENCES

[1] Positite .M. "Omron Beginner's guide to PLC", www.mikrocontrol.co.yu, Serbia, 2003, pp 1-17
[2] Barber Andy, Industrial Mixing, www.foodtechcompare.com, USA,
[3] Bryan .L.A, "Programmable Logic Controllers Theory and implementation", second edition, Industrial Text Company, USA, 1997, pp 4-104
[4] Wikipedia, "Industrial Mixer, www.wikipedia.com/industrial mixer, USA,
[5] Dileep Krishnan, "Intelligent Traffic Light Control using PLC", Cochin University of Science and Technology, India, www.seminarpapers.com,
[6] Gray Richard, "Ladder Logic Programming" Transtronics Inc, USA, www.xtronics.com

[7]Xilinx Inc. 2013. MicroBlaze Soft Processor Core. Retrieved January 23, 2013, from
[8]Welch, J. T., \& Carletta, J. (2000). A direct mapping FPGA architecture for industrial process control applications. Proceedings of the International Conference on Computer Design, pp. 595-598
[9]M. Ikeshita, Y. Takeda, H. Murakoshi, N. Funakubo, and I. Miyazawa, An application of FPGA to high speed programmable controller development of the conversion program from SFC to Verilog, in Proc. 7th IEEE Int l Conf Emerging Technologies and Factory Automation ETFA 99, vol. 2,1999, pp. 1386 1390
[10]D. Gawali, V.K. Sharma, FPGA Based Micro-PLC Design Approach, in International Conference on Advances in Computing, Control, \& Telecommunication Technologies, 2009. ACT '09, Trivandrum, India, December 2009, pp. 660-663.
[11]YASAR BIRBIR,SELCUK NOGAY, "PLC-based Monitoring and Control system for a 3-phase induction Motor", Marmara University, Technical Education Faculty, Turkey, www.csanyigroup.com
[12]D. Cuff, M. Hansen, and J. Kang, "Urban sensing: Out of the woods," Commun. ACM, vol. 51, no. 3, pp. 24–33, Mar. 2008.

