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Exploiting Self Reverse Bias Technique for Low Power SRAM Design

Mr. Rahul. A. Burange[1], Dr. G. H. Agrawal[2]

[1]*Research Scholar, B .D. College of Engineering, Nagpur, burange.rahul@gmail.com*
[2]*Proffessor, K. D. K. College of Engineering, Nagpur, ghagrawal66@yahoo.com*

Abstract- Gated Vdd is one of the techniques to reduce static power in CMOS circuits. Static power dissipation gets drastically reduced by having an extra NMOS transistor between Static RAM (SRAM) cell and ground. This paper exploits the stacking effect by adding multiple NMOS transistors between SRAM cell and ground to reduce the static power consumption further. We examine the effect on power by placing multiple NMOS transistors between SRAM cell and ground. Power analysis is carried out by applying different vectors to the NMOS stack. To reduce the delay added in the SRAM read/write operation as a result of NMOS stack we propose addition of extra transistor in parallel to NMOS stack that is of greater width then the transistors of NMOS stack. Simulation results show that static power gets reduced by approximately 33 % at the cost of 20% increase in area. Simulation results and power analysis of other blocks of SRAM are also presented at the end.

Keywords- SRAM; NMOS; Static Power; Stacking Effect

I. INTRODUCTION

As the number of battery power applications increase, it indirectly puts load on chip designer to reduce circuit power consumption in order to provide more backup for such devices. Microprocessors have large caching structures on chip to ensure availability of data near to CPU registers in order to increase overall speed and performance. These structures consume large amount of power while in operation. The total power dissipated is addition of static and dynamic power consumed by the chip. Until few years ago dynamic power was the majority contributor of the total power dissipation. However in the recent years it was noticed that the static power cannot be neglected and it has become dominant factor of the total power dissipation. Several techniques have been proposed so far for decreasing power dissipation in SRAM [1-3,5-8]. Of these some concentrate on modification in SRAM cell structure [6,11], some are related to architectural changes in the RAM structure like block partitioning and enhancement of supporting circuit [2,3,7,8] while others concentrate on reading and writing techniques to save power [1,10].

The SRAM structure consists of two cross-coupled inverters with two NMOS access transistors that activate the inverter section for read/write operation. Typical SRAM cell is depicted in Fig.1 where Vdd/ Gnd provide operating voltage to the complete cell. Bit line (BL) and Bit line bar (BLB) is used to read/write data into the cell. Word-line (WL) provides access to inverters for storage and retrieval of

data. Other parts of SRAM architecture are pre-charge circuit, sense amplifier, decoders and multiplexers. The structure in Fig. 1 can hold one bit. Hence to create a memory structure, multiple such cells are connected in parallel to form a register. An 8 bit register is depicted in Fig. 2, which consists of 8 cells and can hold up to 8 bits of data. As memory is generally byte addressable, 8-bits are read or written at the same time and hence word-line of these 8 cells are common. However as each cell can hold different bit, bit lines of all cells are driven out separately for data. Bit line bar provides inverted data. Optimization of any parameter at cell level results in overall optimization due to symmetric structures.

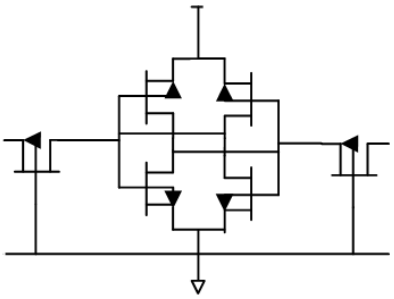

Fig. 1 Conventional 6T SRAM Cell

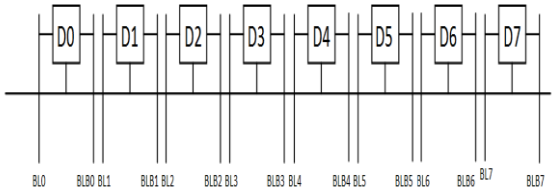

Fig.2 An 8 bit register using SRAM cell

II. LEAKAGE POWER

In CMOS logic the total power dissipation comprises of dynamic and static power. Dynamic power is dissipated during switching of the transistor from high to low or low to high logic and static power gets dissipated while there is no switching i.e. due to the leakage current. During the past years the major factor contributing power dissipation in CMOS circuitry had been dynamic power dissipation [6]. Techniques to reduce dynamic power dissipation have already been explored and implemented [5], as a result of which static power dissipation is becoming the major contributor of total power dissipation. Typical 6 transistor SRAM cell as in Fig. 1 has two access NMOS transistors that are in off state when the data in not being written into or read from the SRAM cell. This is the time when static power gets dissipated in the circuit. A technical report on "**Leakage Power Estimation in SRAMs**" by Mahesh Mamidipaka and others determine the transistors responsible for leakage current during various operational phases.

Here in our research we take into account the power dissipation across such transistors that contribute towards leakage current and calculate the total static power dissipated in the cell. Turning OFF the unused part of RAM or a SRAM cell virtually eliminates all leakage energy dissipation [4]. As in Fig. 1 the source terminal of NMOS of two inverters are short circuited and connected to ground directly. In gated-Vdd technique an NMOS transistor is added that disconnects the ground from the sources of NMOS when the SRAM cell is not in use and hence virtually there is no path for the leakage current to flow. The schematic of SRAM cell with Gated-Vdd is shown in Fig.3. We will refer to this as modified SRAM cell throughout this text. However the added NMOS itself may be responsible for leakage current. Increasing threshold voltage results in reduction in leakage current but also results in large delay [7]. A dual-vt technique described in [2] uses high vt transistors in non critical path to reduce leakage while maintaining performance. The NMOS transistor in modified SRAM cell may be chosen with a higher vt to achieve larger leakage reduction [7].

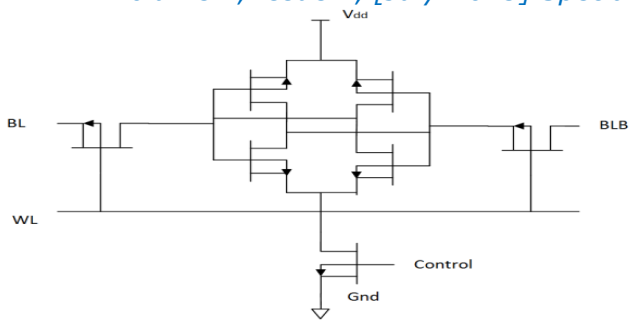

Fig. 3. Gated-Vdd to Reduce Leakage Power

III. STACKING EFFECT

Sub threshold current depends exponentially on VT, VDS and VGS [13]. Therefore it is a function of the terminal voltages, VD,VB,VS and VG. This means that to know sub threshold leakage of a device the biasing condition should be known or by controlling the terminal voltages the sub threshold leakage can be controlled. Input pattern of each gate affects the sub threshold as well as gate leakage current. The leakage of transistors in a stack is a function of no. of transistors and input pattern. Source biasing is the general term for several techniques that change the voltage at the source of a transistor. The goal is to reduce VGS, which has the effect of exponentially reducing the sub-threshold current. Another result of raising the source is that it also reduces VBS, resulting in a slightly higher threshold voltage due to the body effect.

Circuits that directly manipulate the source voltage are rare, and those that exist usually use switched source impedance or a self reversed biasing technique Probably the simplest example of source biasing occurs when "off" transistors are stacked in series. Conceptually, the source voltage of the upper transistor will be a little higher than the source voltage of the lower transistors in the stack. Hence VGS of upper transistor is negative, VBS is negative resulting in increase in threshold voltage and VDS is also lower. Due to this, the leakage of upper transistor reduces [14][15]. This reduction is called stack effect. But this reduction in leakage comes at an increase in delay performance. The reduction in leakage due to stack effect can lead to increase in delay and hence can be used in situations where this delay can be tolerated or by using gates with natural stack [16]. The stack behavior is observed for a 6T SRAM cell by constructing the schematic below for SRAM with gated vdd in the first case (figure 4) and SRAM with NMOS stack for the second case (figure 5).

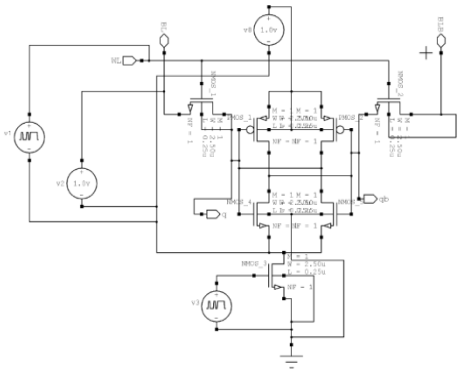

Fig 4. SRAM cell with Gated Vdd

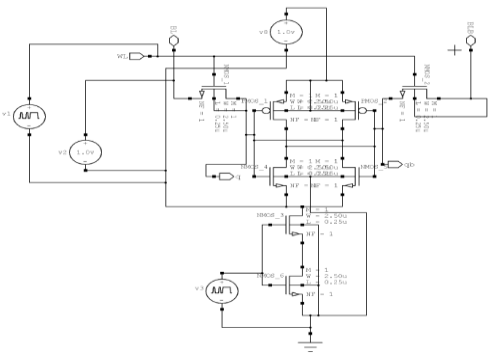

Fig. 5 SRAM cell with NMOS stack

IV. RESULTS

Table 1. Power Results

Technique	Static Power in nW	Power saving compared to no gated-Vdd
No gated-Vdd	15.102	N/A
Gated Vdd, 1 NMOS	13.655	**1.447 nW**
Gated Vdd, 2 NMOS	10.33	**4.772 nW**

The functional verification of the designed cell with respect to the word line and bit line signals is shown in fig.6 below.

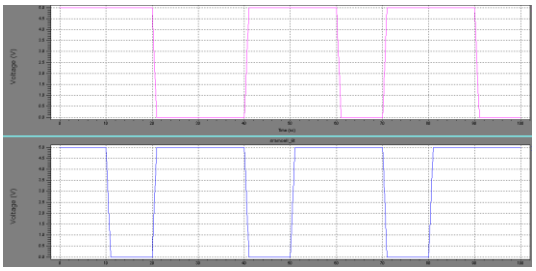

Fig.6 : Functional Verification of SRAM Cell

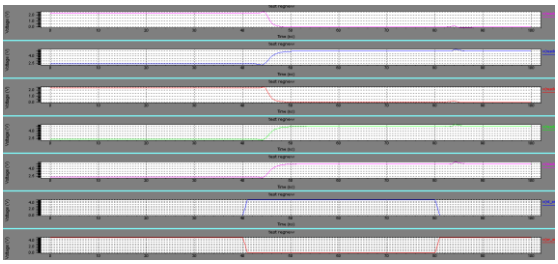

Fig.7 : Simulation of 8 bit SRAM Register

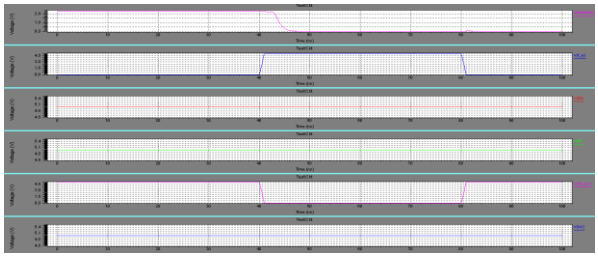

Fig.8 : Simulation of pre-charge circuit.

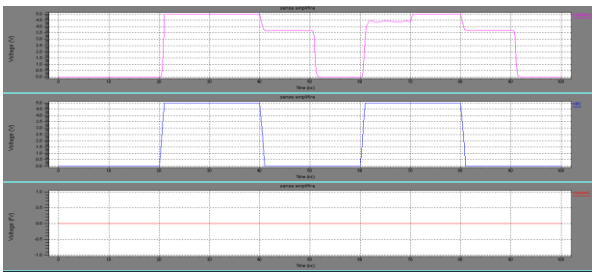

Fig.9 : Simulation of sense amplifier circuit.

V. CONCLUSION

Last column depicts that stacking 2 NMOS results in considerable power saving as compared a single gated NMOS. With the above results we conclude that Stacking effect reduced considerable power compared to conventional Gated-Vdd technique. This power reduction is at the cost of an extra NMOS transistor used in stack. The analysis is carried on a single SRAM cell. As there are millions of cells in Cache memory, the overall power saving will be considerable in the complete structure.

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