

Study of symmetrical and asymmetrical source cascaded Multilevel Inverter

Jyotiprakash Mohaptra¹, Satabdi Das², Dr Bhagabata Panda³

^{1,2,3}Department of Electrical Engg, KIIT University, mohapatra

Abstract—Multilevel Inverter's created level of interest in both industrial application and as well as research areas the new topology of Multilevel inverter produces an important alternative to the classical inverter because of its limitations. In this paper a new class of Multilevel inverter based on "Multilevel DC Link Inverter (MLDCL) topology [1] and a bridge inverter to produce the desired output. In this MLDCL each part having separate DC source which provides stair case output approximating the rectified shape of commanded sinusoidal wave with or without any PWM technique which in later produces an AC output by alternating the polarity. In this paper the limitations made by previous paper was overcome and simulation result in PSIM (9.1.1 version) was shown.

Keywords—Multilevel Inverter, MLDCL, Symmetrical and asymmetrical source, Level generation and polarity generation

I. INTRODUCTION

Recently DC to AC conversion process is growing very rapidly for the area of power electronics, transmission & distribution and utilization of electric power [6]. The application of this are mostly encountered in the area of a less dv/dt, output is distortion less, good voltage & current waveform with most undesirable harmonics eliminated, less switching loss. Now depending upon the output waveform inverter classification are square wave, quasi square wave, two level PWM inverter and multilevel inverter [13]. Particularly MLI's has been introduced for large power and medium voltage applications. The main theoretical aspect behind the MLI structure is to get an output voltage with semiconductor switches to perform the conversion process by synthesizing a stair case voltage waveform which includes a no of DC voltage source. Here capacitors, batteries & renewable energy sources may be used as sources.

1.1 Advantages of Multilevel Inverter

The proposal of multilevel inverter for conversion of DC to AC has following advantages

- This ensures the voltage sharing among active switches which is not easy in the case of two level inverter [2].
- Substantially reduced in size and volume because of elimination of switches.
- It produces an output having better voltage profile with minimum harmonic content.
- Another advantage is instead of GTO we can use IGBT/MOSFET because of its faster switching process and less gate drive requirement as compared to GTO.
- MLI's draw input current with low distortion.
- As MLI's receives a much more attention towards both in topologies and control schemes & it has some limitations-for an increased no of levels we have to use additional switches/sources which may increase the cost, complexity and volume of the circuit.

Generally switches having low rating can be used in MLI & the requirement for each switch are their related gate drive unit, heat sink which will cause the entire system to be costlier. This paper introduces a new type of Multilevel Inverter termed as "Multi Level DC Link Inverter (MLDCL)" and a bridge inverter. The so called new topology of MLDCL has paying a great attention in the academic as well as industry. Analysis of this topology is requires no of semiconductor switches, total voltage blocking capability & requirement, chances of even power distribution amongst the

sources, optimal distribution of switching frequency, possibility of employing both symmetrical & asymmetrical sources.

1.2. Terminology & assessment parameters

1.2.1. Terminology

The various criteria needed to assess the proposed topology is presented below

A. Reduced device count [12]

This topology claims to be used as the less no of semiconductor switches for a given voltage level

B. Voltage blocking capability

Total voltage blocking capability refers to the sum of voltage blocking capability needed for its power switches & is termed as voltage blocking capability.

C. Symmetrical and asymmetrical source configuration [11]

When all the input voltage sources to an Multilevel Inverter are same then it is termed as symmetrical source otherwise it is called as asymmetric. Binary and trinary source configuration are the two examples of asymmetric source configuration. In binary source configuration the value of voltage levels are in geometric progression (GP) with a multiplication factor of 2. Similarly for trinary source the GP factor is 3. In this paper both symmetrical & asymmetrical source configuration are employed.

D. Level generation and polarity generation

Generally Multilevel Inverters produces an output voltage in a stepped form consisting of input DC levels with their additive & subtractive combinations. So the output wave form consists of a no. of levels with both positive & negative half cycles. The part which produces level is termed as level generation & the part which produces polarity is termed as polarity generation part.

1.2.2 Assessment parameters

Merits of this topology is primarily judged based upon the following factors

- The total no of semiconductor switches.
- Total voltage blocking capability.
- The optimal controllability of the topology.
- Possibility of employing symmetrical & asymmetrical source.

II. PROPOSED MLDCL TOPOLOGY

Fig. 1 indicates the schematic diagram of proposed MLDCL topology that contains four input DC sources and eight switches and a single phase full bridge inverter. This has a distinct level generation part & polarity generation part. The part on which levels are created consists of 8 switches ($S_w = 1,2,3,\dots,8$) and the polarity generation part consists of 4 switches ($P_w = 1,2,3,4$). The level generation part synthesizes the DC voltage source $V_{bus(t)}$ connected to the polarity generation part and $I_{bus(t)}$ is the bus current. In the polarity generation part the polarity alternates & produces AC voltage waveform.

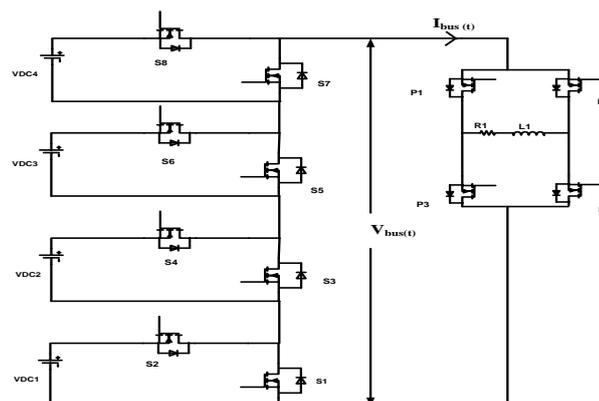


Fig 1. Diagram of MLDCL

In this topology both symmetrical and asymmetrical source of configuration are employed. For symmetrical source the value of source voltage are 10v each while for asymmetrical source the value of voltages are 10V,20V,30V,40V. On comparison with the cascaded topology this topology reduces the no of device count as well as the gate drive units. The various valid switching states are given below

Table 1. Various valid switching states

State	V _{bus(t)}	Switches in ON state
1	VDC,1	S ₂ , S ₃ , S ₅ , S ₇
2	VDC,2	S ₁ , S ₄ , S ₅ , S ₇
3	VDC,3	S ₁ , S ₃ , S ₆ , S ₇
4	VDC,4	S ₁ , S ₃ , S ₅ , S ₈
5	VDC,1 + VDC,2	S ₂ , S ₄ , S ₅ , S ₇
6	VDC,1+ VDC,3	S ₂ , S ₃ , S ₆ , S ₇
7	VDC,1 + VDC,4	S ₂ , S ₃ , S ₅ , S ₈
8	VDC,2 + VDC,3	S ₁ , S ₄ , S ₆ , S ₇
9	VDC,2 + VDC,4	S ₁ , S ₄ , S ₅ , S ₈
10	VDC,3 + VDC,4	S ₁ , S ₃ , S ₆ , S ₈
11	VDC,1 + VDC,2+ VDC,3	S ₂ , S ₄ , S ₆ , S ₇
12	VDC,2 + VDC,3+ VDC,4	S ₁ , S ₄ , S ₆ , S ₈
13	VDC,1 + VDC,3+ VDC,4	S ₂ , S ₃ , S ₆ , S ₈
14	VDC,1 + VDC,2+ VDC,4	S ₂ , S ₄ , S ₅ , S ₈
15	VDC,1 + VDC,2+ VDC,3+ VDC,4	S ₂ , S ₄ , S ₆ , S ₈
16	0	S ₁ , S ₃ , S ₅ , S ₇

It can be easily observed from the table that four switches conduct at the same time for a given level for the level generation and two switches for polarity generation. For the polarity generation switches P1/P2 operates for positive half cycle & P3/P4 operates for negative half cycle and P1, P2/P3, P4 for zero level. The total voltage blocking capability of this topology is minimum which is sum of all the input voltage values. For symmetric source configuration Vdc1=Vdc2=Vdc3=Vdc4=Vdc, it can be observed that the switches need to block a voltage of Vdc & a current equal to the load current. This topology was primarily discussed in [14] on which three phase bridge is used instead of SPFB to reduce the current ripple for BLDC motor.

Generally in the MLDCL the cells provide a staircase shaped DC bus voltage to the SPFB inverter which in turn alternates the voltage polarity to provide an AC voltage of staircase shaped. The relation between the DC bus voltage and current are mentioned below [10]

$$V_{bus(t)} = |V_{dc}| \tag{1}$$

$$I_{bus(t)} = \begin{cases} I_a \text{ for } V_0 > 0 \\ -I_a \text{ for } V_0 < 0 \end{cases} \tag{2}$$

III. SIMULATION AND EXPERIMENTAL RESULTS

To examine the proposed topology simulation has been done for a 1-phase circuit to produce an output of 50 Hz supply. For symmetrical source the output is 40V while for asymmetrical source the output is 100V. The fundamental switching scheme is used to generate gating signals. The experiment has been done on RL load having values 10Ω & 25mH for both symmetrical and asymmetrical source. The THD value for symmetrical source was found to be 15.58 % while for asymmetrical source it is found to be 19.74 %. Simulation diagram and wave forms are shown below

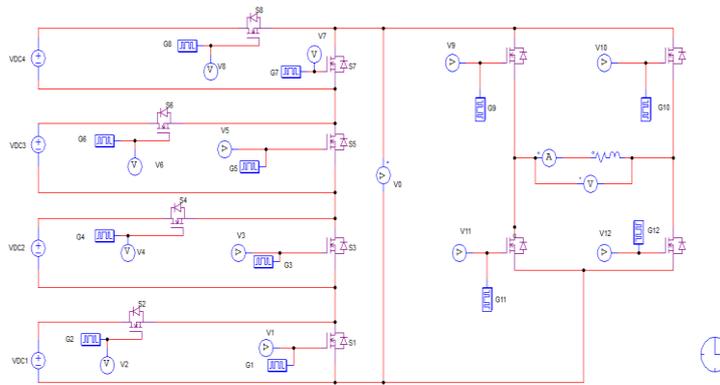


Fig 2. Simulation diagram of MLDCCL

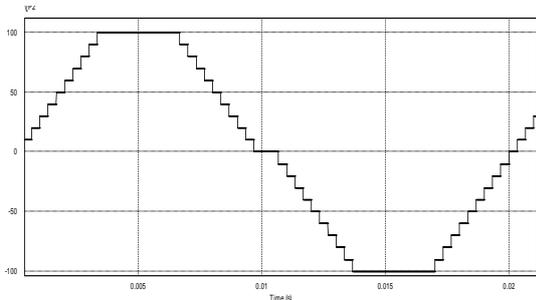


Fig 3. Voltage waveform of asymmetrical source

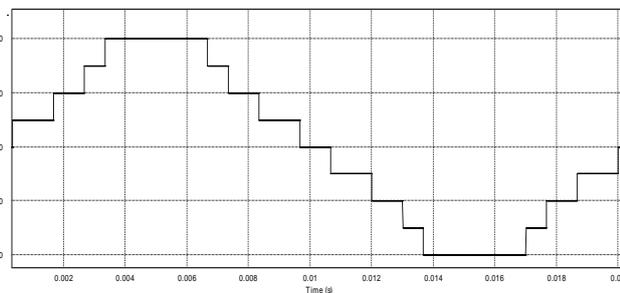


Fig 4. Voltage waveform of symmetrical source

Current wave form for both symmetrical and asymmetrical source are shown below

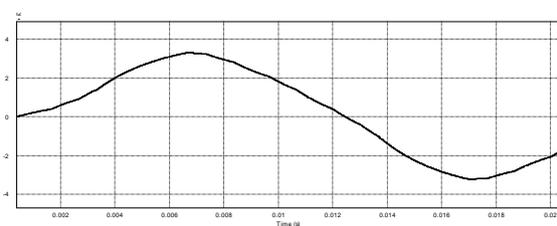


Fig 5. Current waveform of asymmetrical source

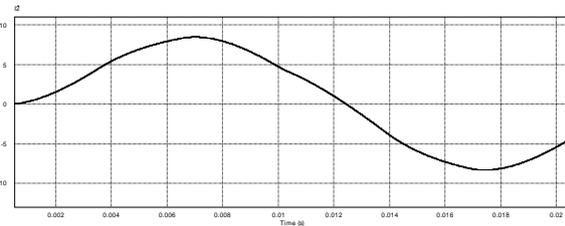


Fig 6. Current waveform of symmetrical source

IV. CONCLUSION

Generally MLI's continue to gain importance in both more power & less power applications so many research persons innovate separate topologies for separate solutions. Also the new topologies are introduced with less no of devices, higher output resolution. In this paper a new topology with developed version was presented. The qualitative & quantitative analysis of MLDCCL was discussed in this paper.

REFERENCES

- [1] K.K.Gupta, Alekh Ranjan, Pallavee Bhatnagar and Shailendra Jain "Multilevel Inverter with reduced device count-A review" in IEEE Trans. on Power electronics, 2015
- [2] Espinoza, J.R and M.H. Rashid "Inverters", Power Electronics Handbook pp 225-269,
- [3] Abbott, D. "Keeping the energy Debate clean : How do we supply the worlds energy needs" in Proceedings of the IEEE, vol. 98, no. 1, pp. 42-66, Jan 2010
- [4] Gui-Jia Su, " Multilevel DC Link Inverter " in IEEE, pp 806-812, 2004
- [5] E.Najafi, AHM Yatim, "Design and Implementation of a new Multilevel topology", in Industrial Electronics, IEEE Transaction, Vol.59, no.11, pp.4148-4154, Nov.2012
- [6] G.madhu sagarbabu, Mr.G.Durga Prasad and Dr.V.Jagathesan "Multilevel DC link inverter topology with less no of switches", in Advance in Electronics & Electric engg., vol.4, pp-67-72,2014
- [7] R.H.Baker, "Bridge converter circuit", in U.S. Patent, vol.4, pp.-163-270,May 1981

- [8] J.S.Lai, F.Z.Peng, "Multilevel converter-A new breed of power converters", in IEEE/IAS Annual meeting,pp.2348-2356,Oct.8,1995
- [9] J.Rodriguez,L.G. Franquelo, S.KOuro, J.I. Leon, R.C.Portillo,M.A. Perez "Multilevel converters-An enabling technology for high power application", in proceedings of IEEE, vol.97, no.11, pp.1786-1817,Nov.2009
- [10]M.A.Parez, P.Cortes, J.Rodreguez, "Predictive Algorithm Technique for Multilevel asymmetric cascaded H-bridge inverter", in Industrial Electronics, IEEE transaction,vol.55, no.12, pp.4354-4364, Dec.2008
- [11]P.Lezena, J.Rodriguez, D.A. Oyarzun, "Cascaded Multilevel inverter with Regeneration Capability & Reduced no of switches", in Industrial electronics,IEEE transaction,vol.55,n0.3,pp.1059-1066,March 2008
- [12]Daher, S. "Analysis, design and implementation of a high efficiency Multilevel converter for renewable energy system", PhD dissertation, 2006
- [13]G.J.Su and D.J.Adams "Multilevel DC Link Inverter for Brushless Permanent motor with very low inductance" in IEEE/IAS annual meeting,vol.2,pp.829-834,sept.3-2012