An Efficiency of Resonant dual active bridge topology

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ABSTRACT-This work presents a new resonant dual active bridge (DAB) topology, which uses a tuned inductor–capacitor–inductor (LCL) network. In comparison to conventional DAB topologies, the proposed topology significantly reduces the bridge currents, lowering both conduction and switching losses and the VA rating associated with the bridges. The performance of the DAB is investigated using a mathematical model under various operating conditions. Experimental results of a 2.5-kW prototype, which has an efficiency of 96% at rated power, are also presented with discussions to demonstrate the improved performance of the tuned LCLDAB topology.Results clearly indicate that the proposed DAB topology offers higher efficiency over a wide range of both input voltage and load in comparison to conventional DAB topologies.

Keywords- DAB topology, resonant network, LCL network

I. INTRODUCTION

In recent years, global concerns regarding future fossil fuel shortages have spurred efforts to reduce the reliance on oil, coal, and gas to generate electricity. Consequently, electricity is increasingly generated from solar, wind, or tidal energy sources. These sources are renewable in nature, but highly variable, leading to the possibility of significant dynamic mismatches between electricity supply and demand levels[3,4]. How- ever, it has been proposed that the degree of mismatching can be reduced through integrating the batteries of electric vehicles (EVs), whicharenotbeingusedatanygiventime,intonational electric grid. This would provide a means for dynamic grid stabilization, but requires a bidirectional power interface between thegridandEVstoallowvehicle-to-grid(V2G)energy transfers to take place[1,2]. Amongthemany typesof bidirectional dc–dc converters that couldbeusedinaV2Gsystem,theDABconverterisapreferred option, as it has a small component count, offers isolation, and allows for high power operation[5]. In addition, it has the ability to accommodate a wide range of voltage levels, as it may be controlled to operate in buck or boost modes. However, a conventional DAB converter using single phase-shift (SPS) control draws a large reactive current component at low operating power levels, which increases theconverter conduction losses[6,7]. This current component also necessitates the use of a larger dc-link capacitor. Therefore, various techniques
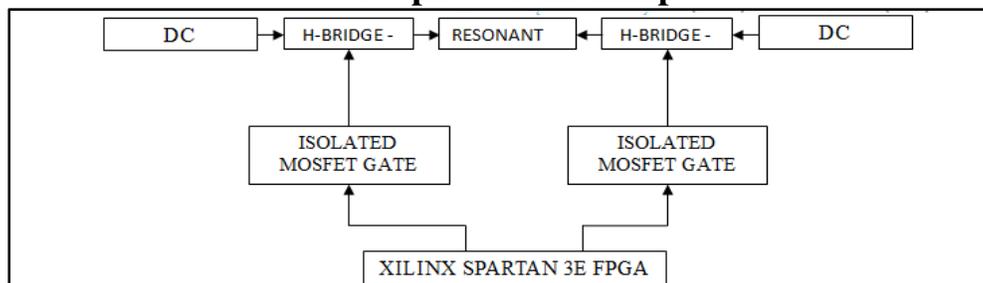
II.Experimental setup

Fig 1: Experimental setup for DUAL active bridge topology

2.1. Bridge rectifier

A single-phase half-wave rectifier consists of a single diode connected. This is the simplest of the rectifier circuits. It produces an output waveform that is half of the incoming AC voltage waveform. The positive pulse output waveform occurs because of the forward-bias condition of the diode. A diode experiences a forward-bias condition when its anode is at a higher potential than its cathode. Reverse bias occurs when its anode is lower than its cathode. During the positive portion of the input waveform, the diode becomes forward biased, which allows current to pass through the diode from anode to cathode, such that it flows through the load to produce a positive output pulse waveform. Over the negative portion of the input waveform, the diode is reverse- biased ideally so no current flows. V_P(in) is the peak value of the input voltage waveform and VF is the forward-bias voltage drop across the diode. This output voltage is used to determine one of the specification values in the selection of a diode for use in a half-wave rectifier. Other voltage and current values are important to the operation a

Half-wave rectifier circuit using a transformer with a 14:1 turns ratio to step down the line voltage of 120 V-rms to 12 V-peak. It consists of a transformer with a 14:1 turns ratio, a single diode D1 of the commercial type 1N4148, and a load resistance 'R' load of 1 k Ohm. The source resistance of 0.5 Ohm of the AC line is also included in this circuit. The purpose of the transformer is to step down the main household AC power supply voltage of 120 V-rms to a 12 V-peak level. Spice does not make provision for an ideal transformer, probably for a good reason; one does not exist in practice. Instead, Spice allows coupled inductors to be described having a coefficient of coupling k less than one. Two inductors, say for example, LP and LS, which share a common magnetic path and have a coefficient of coupling k very close to unity, say 0.999, would be a reasonably good model of many practical transformers.

2.2. Electronic filter

Fig 2: Real time picture of Electronic filter

Television signal splitter consisting of a high-pass filter (left) and a low-pass filter (right). The antenna is connected to the screw terminals to the left of center.Electronic filters are electronic circuits which perform signal processing functions, specifically to remove unwanted frequency components from the signal, to enhance wanted ones, or both. The most common types of electronic filters are linear filters, regardless of other aspects of their design. See the article on linear filters for details on their design and analysis.The output filter constitutes the last element of the inverter circuit. It takes the sinusoidal output PWM generated and passed through the bridge and filters it so that it is now usable across any electronic devices. It also allows us to output a real pure sine wave with less distortion and little attenuation by performing digital processing functions, removing undesired frequency components

on the signals, and also using wanted ones or both. In fact, we can distinguish low pass filter, high pass filter, and band pass filter.

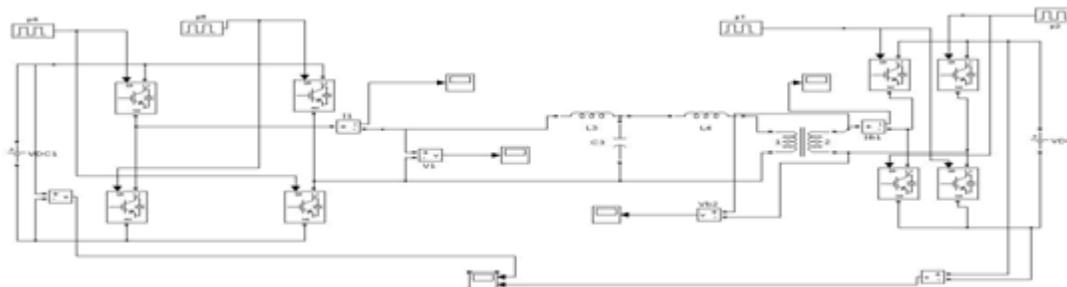## III. SCHEMATIC REPRESENTATION OF THE CIRCUIT DIAGRAM

Fig 3 : Schematic representation of circuit diagram

This work, therefore, proposes DAB topology, which utilizes a resonant network to minimize the reactive power requirement of the converter over the entire load range. The proposed converter employs a tuned inductor–capacitor–inductor (LCL) network, which includes the leakage inductance of the isolation transformer, to significantly reduce the magnitude of bridge currents and, therefore, the switch and copper losses. A simple control scheme is employed, where each bridge is driven with equal PWM while maintaining the phase shift between the bridges fixed at 90◦ or −90◦, to regulate the direction and magnitude of power flow. Theoretical analyses as well as simulated results are presented in comparison with experimental evidence of a 2.5-kW prototype system, demonstrating the ability of the proposed topology to transfer bidirectional power at a high efficiency over a wide range of power and dc supply voltages.

IV. CONFIGURATION MODES OF THE FPGA

The FPGA controls the FLASH device through a reset and clock pin. In this mode, there are no addresses that need to be issued by the FPGA.In contrast, Parallel load with FPGA as master uses addresses.Here, the FPGA maintains an internal counter that generates the byte addresses. The advantage is reduced configuration time and off-the-shelf memory chips. However, in the early days, the fetched byte was serially clocked into the scan chain, so it wasn't faster. Similar to serial mode, these pins can be reused as general purpose I/O's. Unfortunately, this is not often used because of the load associated with the hard-wired memory device.
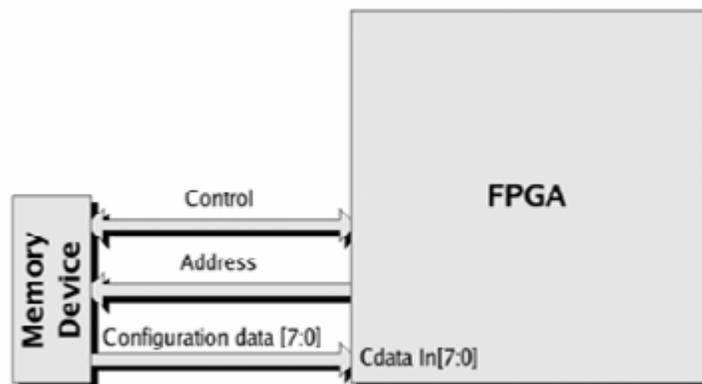

FIG 4.Parallel loads with FPGA

4.1. FPGA design flow

FPGAs are RAM based. They need to be "downloaded" (configured) at each power-up. CPLDs are EEPROM based. They are active at power-up (i.e. as long as they've been programmed at least once...).CPLDs have a faster input-to-output timings than FPGAs (because of their coarse-grain architecture, one block of logic can hold a big equation), so are better suited for microprocessor decoding logic for example than FPGAs.FPGAs have special routing resources to implement efficiently binary counters and arithmetic functions (adders, comparators...) and RAM. CPLDs do not.FPGAs can contain very large digital designs, while CPLDs can contain small designs only.
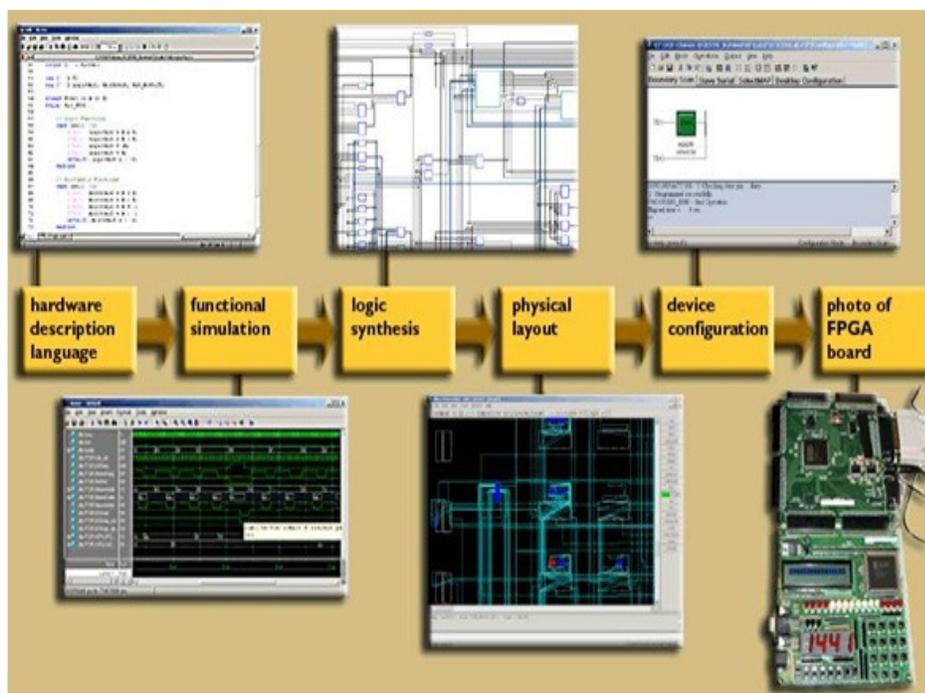

Fig 5: FPGA Design Flow

Transceiver need to receive the command to control the motor,therefore the input command is given user interface which is PC. The data given by the user gets transmitted byZigbee wireless communication as shown in block diagram FPGA is connected with the Thyristor driver that controls the gate triggering of Thyristors in the controlled rectifier. Then finally the controlled rectifier controls the speed of motor. Upon the reception of appropriate command issued by the user, it transmits motor's speed and current firing angle of controlled rectifier circuitry to the FPGA.Data are interchanged through Zigbeetransceiver that provides easy and precise control over the machine.

V. SIMULATION STUDY

This part of MATLAB is the set of tools and facilities that help you use and become more productive with MATLAB functions and files. Many of these tools are graphical user interfaces. It includes: the MATLAB desktop and Command Window, an editor and debugger, a code analyzer, and browsers for viewing help, the workspace, and folders. This library is a vast collection of computational algorithms ranging from elementary functions, like sum, sine, cosine, and complex arithmetic, to more sophisticated functions like matrix inverse, matrix eigenvalues, Bessel functions, and fast Fourier transforms.

5.1 Accelerator Mode and Real-Time Workshop Software

The Simulink Accelerator mode is explained in the Accelerating Models documentation.The Accelerator mode speeds up the execution of Simulink models by replacing the interpreted M code running beneath the Simulink blocks with compiled code as your model executes. The Accelerator mode uses portions of Real-Time Workshop$^®$ software to generate this code on the fly. Although the Accelerator mode uses this technology, Real-Time Workshop license is not required to run it. Also, if you do not have your own C compiler installed, you can use the LCC compiler provided with your MATLAB installation. To activate the Accelerator mode, select Accelerator from the Simulation menu of your model window. Alternatively, you can select Accelerator from the pull-down menu in the model window toolbar.The following table 1 shows typical performance gains obtained with discretization and Accelerator mode applied on the following two demos: a DC drive using a chopper and the AC-DC converter using a three-phase, three-level voltage-sourced converter. Two versions of the DC drive model are provided as demos shipped with the product: a continuous version, power_dcdrive, and a discrete version, powered drive disc. The AC-DC converter is available as the power_3levelVSC demo. The table shows how discretizing your circuit speeds up the simulation by a factor of 1.33 for the DC drive. Using the Accelerator mode, an additional factor of 1.7 performance gain is obtained. For the AC-DC converter the Accelerator mode provides a gain of 4.4 times. For complex power electronic converter models, the Accelerator mode provides performance gains up to factors of 15.To take full advantage of the performance enhancements made possible by converting your models to code, you must use Real-Time Workshop software to generate stand-alone C code. You can then compile and run this code and, with xPC Target™ software, also run it on a target PC operating the xPC Target real-time kernel.

Simulation Method	Simulation Time in Seconds*	
	DC drive (Stop time = 2 s)	AC-DC converter (Stop time = 0.2 s)
Continuous: ode23tb default parameters	12	—
Discrete	9.0 (Ts = 10 µs)	14.5 (Ts = 5 µs)
Discrete + Accelerator	5.2 (Ts = 10 µs)	3.3 (Ts = 5 µs)

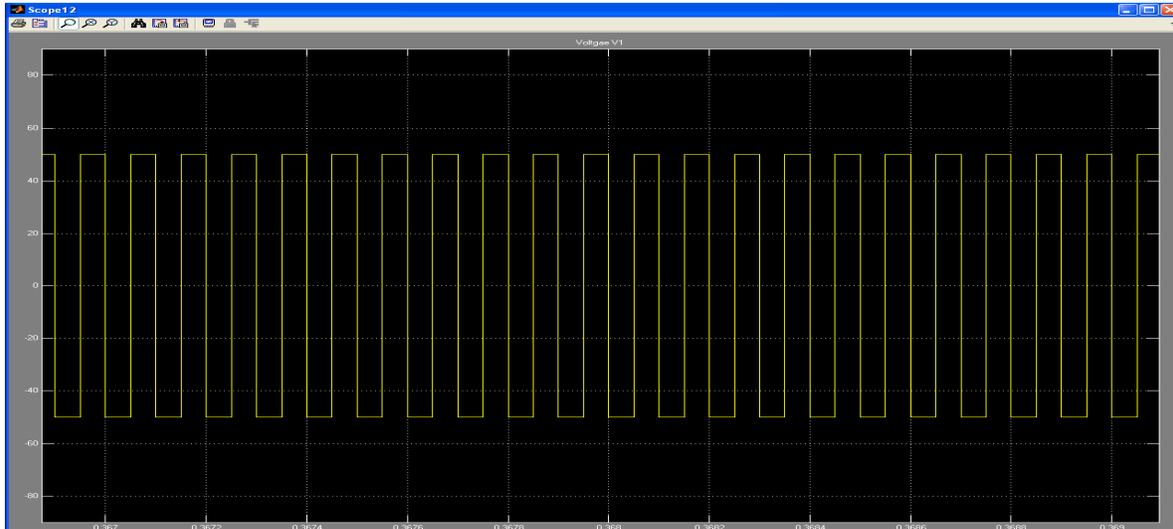Table 1: Simulation times obtained on a Pentium IV 2.6 GHz processor

Fig 6: Switching pulse

5.2 Changing Circuit Parameters

As for the Simulink blocks, all the **powerlib** library block parameters that you specify in the dialog box can contain MATLAB expressions using symbolic variable names. Before running the simulation, you must assign a value to each of these variables in your MATLAB workspace. This allows you to perform parametric studies by changing the parameter values in a MATLAB script.
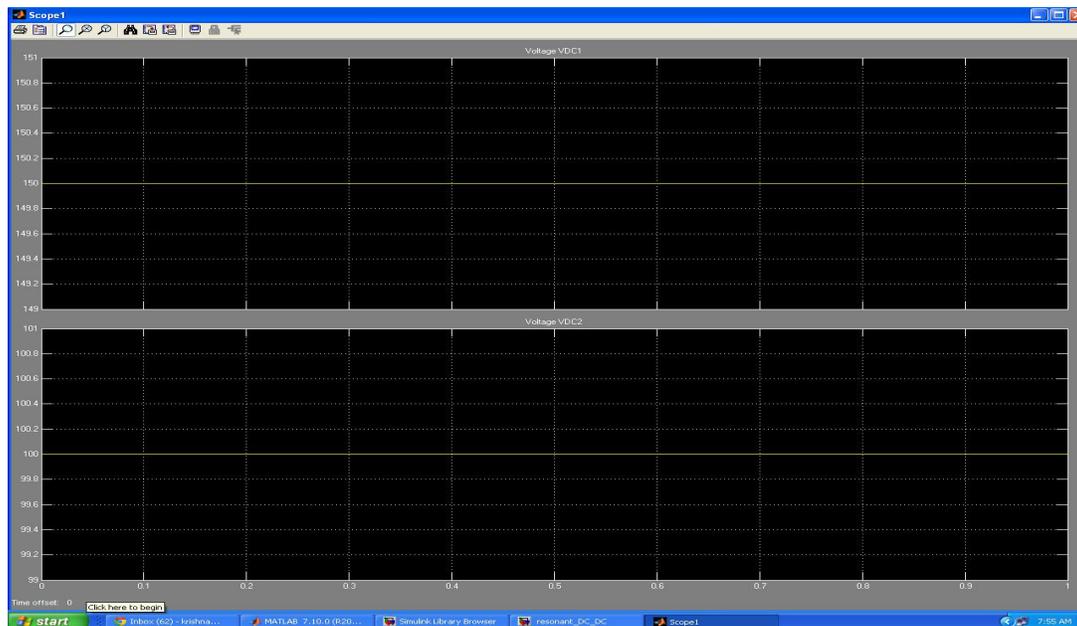

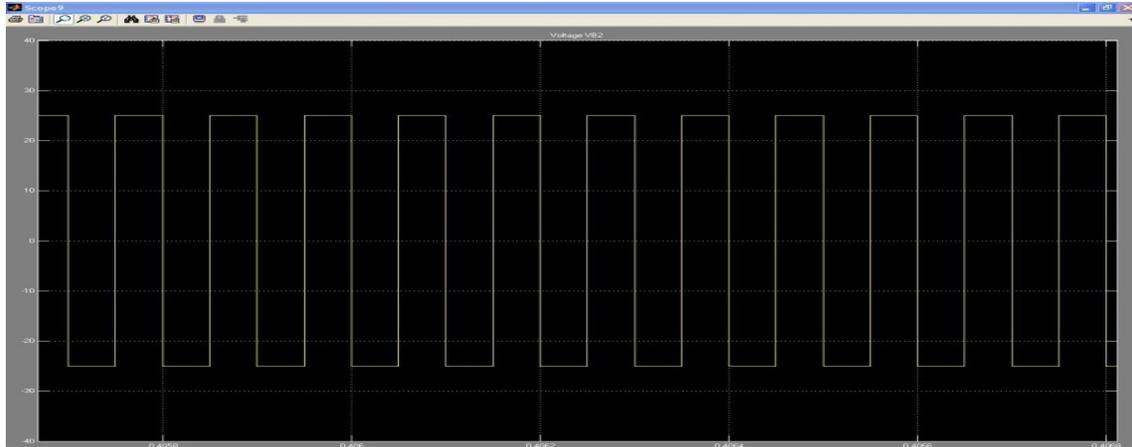Fig 7: Input voltage pulse

Fig 8: Output pulse

VI. Conclusion

A new dual DAB topology that employs an LCL resonant network has been described. A mathematical model has been presentedtoaccuratelypredicttheperformanceoftheproposed topology.Experimentalresultsofa2.5-kWprototypeDAB, operated under various conditions, have also been presented to demonstrate the improved performance of the converter. Results indicate that the proposed DAB topology has lower bridge currentsand,consequently,offershigherefficiencyoverawider supply voltage and load range in comparison to conventional DAB topologies.

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