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Design and Implementation of 8x8 VEDIC Multiplier Using Submicron Technology

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Abstract— Multiplication is one of the basic operations for any high speed digital logic system design, digital signal processors or communication system. Primary issues in design of multiplier are area, delay, and power dissipation. There are many algorithms like booth multiplier, array multiplier, vedic multiplier, compressor based vedic multiplier for overcoming this problems. This paper mainly presents VEDIC multiplier using Urdhva Tiryagbhyam Sutra and it uses Full Adder, Ripple Carry Adder, and basic gates. Keeping in mind that power dissipation and delay are the primary factors for multiplier and it should be improved in the design. The design has been implemented using 45nm CMOS technology at 1.0v supply voltage in LTSpice IV tool. The results are compared with previously reported papers.

Index Terms — Vedic Multiplier, Urdhva Tiryagbhyam Sutra, CMOS 45nm Technology, Ripple Carry Adder, Simulation Results, Comparison.

I. INTRODUCTION

Multiplier is one of the common operations that is widely used in many digital signal processors, communication systems, encryption and decryption algorithms. A general multiplier block consists of AND gates to generate the partial products and ADDERS to add these partial products. But as the number of bits that are to be multiplied increases, the need for ADDER blocks increase. This would in turn result in a delay due to long ADDER tree structure. Besides this power consumption by the typical multiplier is also the major issue that needs to be concerned.

Thus, to eliminate these problems the nonconventional ancient method of Vedic mathematics has been adopted in this paper.

The Vedic mathematics comprises of 16 different Vedic sutras called Vedic formulae, which are used to solve a wide range of mathematical problems. These sutra save a lot of time as compared to conventional computations.

The 16 Vedic mathematics formulae are as follows:

- Shunyamanyat – If one is in ratio, the other is zero
- Chalana-Kalanabyham – Differences and Similarities.
- Ekadhikina Purvena – By one more than the previous one
- Ekanyunena Purvena – By one less than the previous one
- Gunakasamuchyah – The factors of the sum is equal to the sum of the factors
- Gunitasamuchyah – The product of the sum is equal to the sum of the product
- Nikhilam Navatashcaramam Dashatah – All from 9 and the last from 10
- Paraavartya Yojayet – Transpose and adjust
- Puranapuranabyham – By the completion or noncompletion
- Sankalana-vyavakalanabhyam – By addition and by subtraction
- Shesanyankena Charamena – The remainders by the last digit
- Shunyam Saamyasamuccaye – When the sum is the same that sum is zero
- Sopaantyadvayamantyam – The ultimate and twice

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- Urdhva-tiryagbyham – Vertically and crosswise
- Vyashtisamanstih – Part and Whole
- Yaavadunam – Whatever the extent of its deficiency

This paper proposes 8x8 Vedic multiplier using Urdhva Tiryagbhyam sutra of Vedic mathematics and uses CMOS 45NM technology which is implemented in LTSpice IV tool. The rest of paper is organized as follows. Section II gives the methodology of Vedic multiplication technique. Section III gives the proposed multiplier architecture. Section IV gives the schematic and simulation of the multiplier. Section V gives result, its comparison with previously reported papers and conclusion.

II. VEDIC MULTIPLICATION METHOD

The use of Vedic mathematics provides reduced calculations and reduced delay in conventional mathematic problems. This is because the Vedic mathematics is based on the principles on which algorithms are implemented as human minds interpret.

Out of 16 Vedic sutras given by ancient mathematics, the formulae which are being used for the purpose of multiplication are 1) Nikhilam Navatashcaramam Dashatah – All from 9 and the last from 10 and 2) Urdhva-tiryagbyham – Vertically and crosswise.

A. Urdhva Tiryagbhyam Sutra

As the multiplication operation in UT sutra is computed parallel the delay in output is significantly reduced. The sutra is also known as 'vertically and crosswise'. Initially the UT sutra was used for decimal numbers only. However it can also be used for binary numbers. The method how binary multiplication is done using UT method for 2-bit, 3-bit and 4-bit numbers is shown in Figure 1.

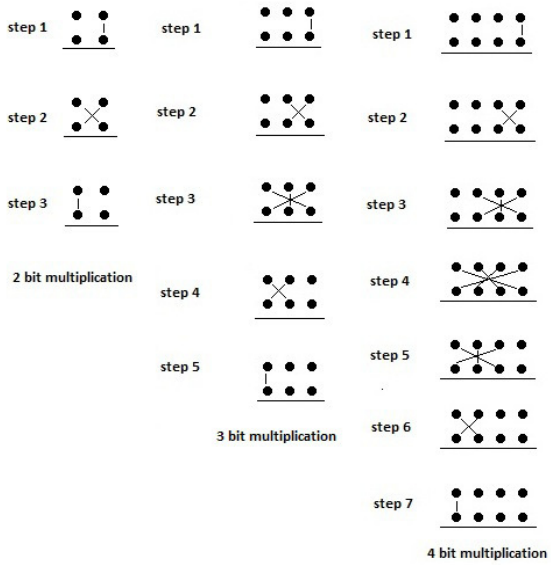

Figure 1. UT Method for 2,3,4 bit numbers

Since the partial products and their sums are calculated independently, the multiplier is independent of the clock of the processor. The delay is generated only due to the occurrence of carry from the partial products which is needed to be added in each next step's partial product.

B. Multiplication of two decimal numbers 252 x 846

To understand the working of UT method, let us consider the multiplication of two decimal numbers 252 x 846 as shown in Fig. 2. Initially the carry is taken as zero and the multiplication is done vertically for least significant bit. It generates a result. Result is added to initial zero carry and this generates one bit result and one pre-carry. The next step is crosswise multiplication. The result of crosswise multiplication is again added with pre-carry to generate one bit result and pre-carry for the

next step. Thus the process continues. In genral, least significant bit acts as the result bit and all other bits act as carry for the next step.

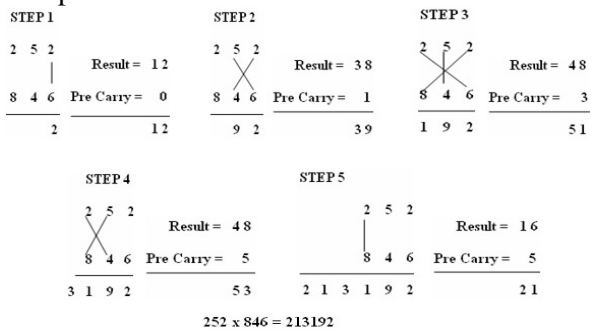

Figure 2. Multiplication of 252x846

III. PROPOSED MULTIPLIER ARCHITECTURE

The proposed architecture for 2X2, 4x4 and 8x8 bit Vedic multiplier are shown in the below sections. Here, "Urdhva-Tiryagbhyam" (Vertically and Crosswise) sutra is used to for the multiplication of two binary numbers. The idea behind use of Vedic multiplier is that the partial product generation and additions are done simultaneously. Hence, it is equivalent to parallel processing. This characteristic makes it more attractive for binary multiplications. This in turn reduces delay, which is the primary motivation behind this work.

A. 2x2 bits Vedic Multiplier

Consider the following two, 2 bit numbers A and B where A = a1a0 and B = b1b0 as shown in Fig. 3. Firstly, the least significant bits a0 and b0 are multiplied which gives the least significant bit s0 of the final product (vertical). Then, the LSB of the multiplicand is multiplied with the next higher bit of the multiplier and added with, the product of LSB of multiplier and next higher bit of the multiplicand (crosswise). The sum gives second bit s1 of the final product and the carry is added with the partial product obtained by multiplying the most significant bits to give the sum s2 and carry c2. The sum is the third corresponding bit and carry becomes the fourth bit of the final product.

s0 = a0b0…….. (1)
c1s1 = a1b0 + a0b1……... (2)
c2s2 = c1 + a1b1……..... (3)

The final result will be c2s2s1s0. This multiplication method is applicable for all the cases.

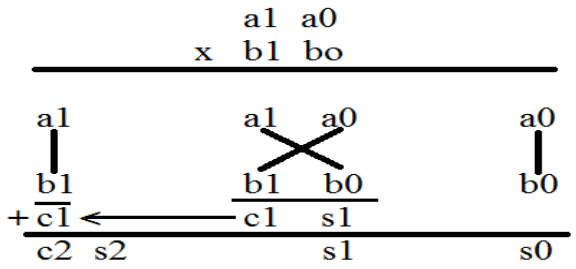

Figure 3. Multiplication of two binary numbers A & B

Equations (1), (2) and (3) show that the 2X2 multiplier requires four AND gates & two half-adders which is displayed in its block diagram in Fig. 4. By observation it is seen that the conventional multiplier would do the same process of multiplying LSB and MSB of multiplicand to multiplier and adding them to generate result. Thus there is not any significant amount of

improvement in efficiency of Vedic multiplier. So we switch to the implementation of 4x4 bit Vedic multiplier using 2x2 bit multiplier as a basic building block. The same method can be applied for extending 8x8 bit multiplier from 4x4 multiplier. But for higher no. of bits in input, there are some changes required.

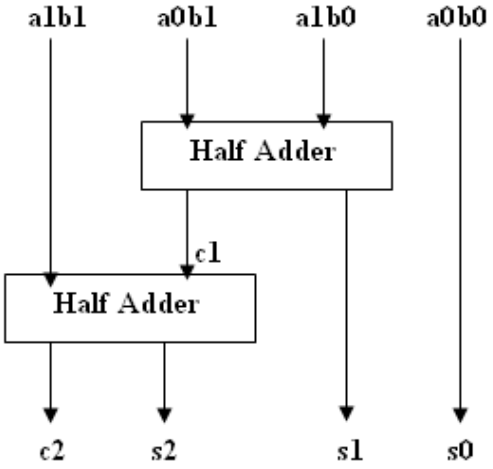

Figure 4. Block Diagram of 2x2 Multiplier

B. Vedic Multiplier for 4x4 bit Module

The 4x4 bit Vedic multiplier is implemented using four 2x2 bit Vedic multiplier blocks as discussed in Fig. 6. Let's assume the two 4 bit numbers, say A= A3 A2 A1 A0 and B= B3 B2 B1 B0. The output line for the multiplication result is – S7 S6 S5 S4 S3 S2 S1 S0. Divide A and B into two parts, say A3 A2 & A1 A0 for A and B3 B2 & B1 B0 for B. Now assume two bits together and consider it a single bit then, the number of bits to be multiplied will be now 2x2. The multiplication results will be 4 bits which are composed of two bits together and their separate multiplication is to be done using 2x2 multiplier, which is shown in the figure 5.

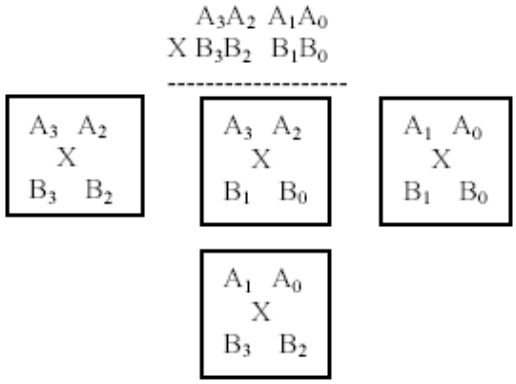

Figure 5. Block Diagram of 4x4 multiplier

Each block is made up of 2x2 bit Vedic multiplier. First 2x2 bit multiplier inputs are A1A0 and B1B0(Vertically). The last block is 2x2 bit multiplier with inputs A3A2 and B3B2(Vertically). The middle two 2x2 bit multipliers with inputs A3A2 & B1B0 and A1A0 & B3B2(Crosswise). So the final result is of 8 bit, S7 S6 S5 S4 S3 S2 S1 S0. To see the bit by bit configuration, the Block diagram of 4x4 bit Vedic multiplier is shown in Fig. 5. To get final result of multiplications (S7 S6 S5 S4 S3 S2 S1 S0), four 2x2 bit Vedic multipliers and three 4-bit Ripple-Carry (RC) Adders are necessary. The proposed Vedic multiplier can be used to reduce delay. Literature review has shown that earlier multipliers were based on array multiplier structures. On the contrary, we proposed a new architecture, which is more efficient in terms of speed. The RC Adders are made up of full adders,

which help us to reduce delay. Similarly, 8x8 Vedic multiplier modules can be implemented easily by using four 4x4 multiplier blocks.

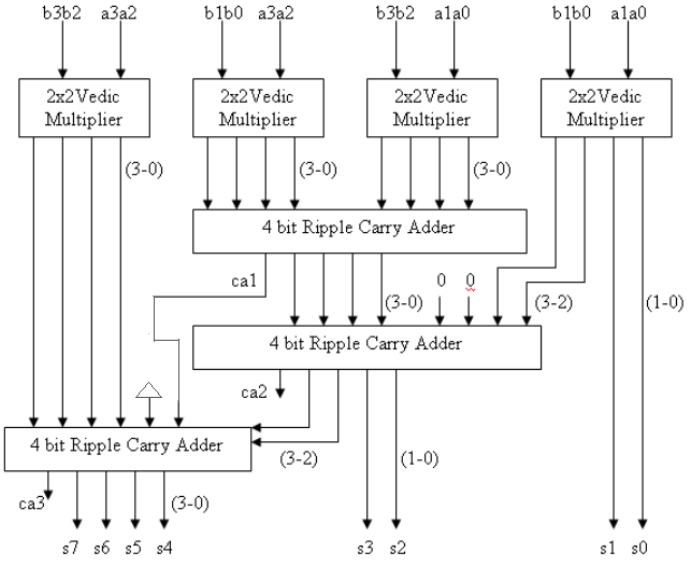

Figure 6. 4x4 Multiplier Architecture

C. Vedic Multiplier for 8x8 bit Module

The 8x8 bit Vedic multiplier can be easily implemented by using four 4x4 bit Vedic multiplier blocks as shown in the block diagram in Fig. 7 which was discussed in the previous section. Let's assume two numbers for 8x8 multiplications, say A= A7 A6 A5 A4 A3 A2 A1 A0 and B= B7 B6 B5 B4 B3 B2 B1B0. In multiplication result the output bits will be of 16 bits as – S15 S14 S13 S12 S11 S10 S9 S8 S7 S6 S5 S4 S3 S2 S1 S0. Now assume A and B into two parts, say the 8 bit multiplicand A is made of 4 bits AH-AL each. Similarly multiplicand B is made of two parts of 4 bits BH-BL respectively. The 16 bit result can be given as: P = A x B = (AH-AL) x (BH-BL) = AH x BH + (AH x BL + AL x BH) + AL x BL

Using the fundamental of Vedic multiplication, taking four bits at a time and using 4 bit multiplier block as discussed we can perform the multiplication. The outputs of 4x4 bit multipliers are added accordingly to obtain the final product. Here total three 8 bit Ripple-Carry Adders are required as shown in Fig 7.

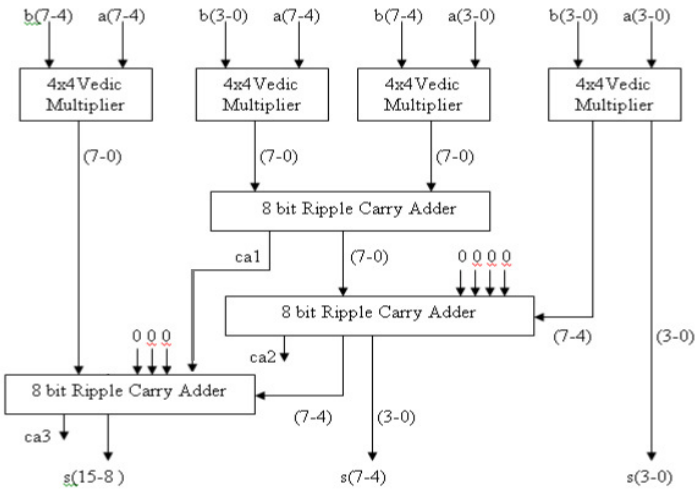

Figure 7. Architecture of 8x8 multiplier

IV. 8X8 BIT MULTIPLIER SCHEMATIC AND SIMULATION

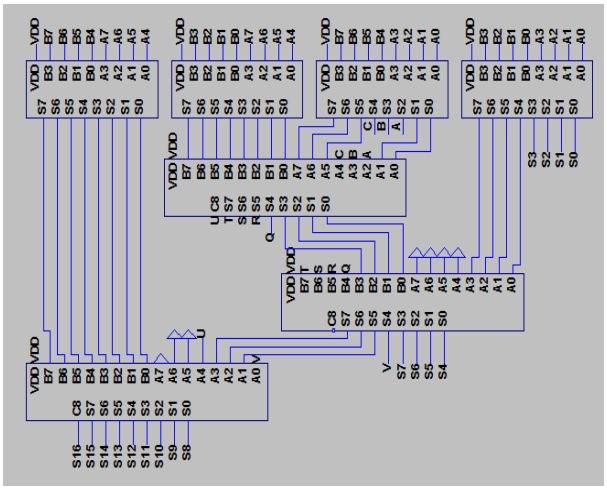

Figure 8. Schematic of 8x8 mul. in LTSpice

V. COMPARISONS OF 8X8 BIT VEDIC MULTIPLIER WITH PREVIOUS DESIGNS AND CONCLUSION

The proposed Vedic Multiplier is designed with the new CMOS technology and it architecture become successful for the delay, power dissipation and area means number of transistors

Table 1. Comparisons of 8x8 Bit Vedic Multiplier with Previously Designed Multipliers

Parameters	**Proposed Design**	**[10]**	**[8]**	**[1], [7]**	**[6]**	**[2]**
VDD	1V	1V	-	2.5-5V	1.8V	3.5V
Delay	634.544 (ps)	0.635 (ns)	4.53 (ns)	-	0.95 (ns)	1.21 (ns)
Power	764.32 uW	7.46 uW	4.86 mW	93.86 mW	16 mW	8.08 mW
Technology	45 nm	45 nm	350 nm	180 nm	180 nm	350 nm

In this paper, a deep detailed study of 8x8 bit Vedic Multiplier is carried out. Multiplier very important in DSP (Digital Signal Processing) and Math processors so it should be faster and here tried to make this thing possible. The design has been implemented using PTM 45nm CMOS technology at 1.0v supply voltage in LTSpice IV tool. Also it has very low power dissipation compared to other Multipliers because in Vedic Multiplier the partial products were generated independently which is much faster than conventional partial product generation. The power dissipation of 0.764 mW and a delay of 634.544 ps has been observed for Proposed 8x8 bit Vedic Multiplier. This achieved result was good than previously reported papers.

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