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A MODIFIED SINGLE STAGE AC-DC CONVERTER USING PWM SCHEME WITH FPGA CONTROLLER

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Abstract—In this paper, a modified single stage ac-dc converter using pwm scheme with field programmable gate array (FPGA) controller. This converter integrates the operation of the corrected power factor at input side and ac-dc converter operation. This ac-dc converter is made to operate with FPGA controller for regulated dc output voltage. A center tapped transformer is connected to the input through only two diodes, which results in low conduction losses. Equations and configurations are given to design for the transformer. This converter is operating with two controllers with FPGA. One controller that performs power factor correction and other controller that regulates dc output voltage. The paper explains the operation of the new converter in detail and discusses its features and a procedure for its proper design. Experimental results obtained from a prototype are presented to confirm the feasibility of the new converter.

Keywords— pulse width modulation (PWM), Field-programmable gate array (FPGA), AC-DC voltage conversion, hardware description language (HDL).

I. INTRODUCTION

A Modified single stage ac–dc converters using PWM scheme with FPGA are required to have some sort of power factor correction (PFC) capability to comply with harmonic standards such as IEC61000-3-2. Modified single stage ac-dc converter consisting of bridge rectifier and switching circuit at their input stage have been generally used. Input current harmonics cause the poor power quality network. Furthermore, power generation facilities should be increased in order to supply a large instant power that occurs near the peak of the line voltage. To reduce the harmonics, one of the most widely used methods is the boost topology operating conduction mode followed by a dc-dc converter. It shows good performance such as high power factor and fast output voltage regulation but increases cost and size due to additional semiconductor switches and control circuits. But reduced cost of modified ac-dc converter using PWM scheme with FPGA controller compared to ac-dc fly back boost converter.

A modified single stage converter with FPGA draw a high quality line current waveform through discontinues conduction mode operation and has a single stage, small number of MOSFET switches. Although it has simple structure, this approach has undesirable features. This is because only a single stage exists for the output dc voltage regulation and the dc bus voltage is determined by the capacitor charge balancing. But fly back converter or other single stage converters suffer from this problem, which has more number of capacitors. So its need more capacitor banks. Modified single stage ac-dc converter with FPGA has two capacitors only. Two transformers using for other single stage, two stage converter and fly back boost converters. The proposed converter has only one of the centre tapped transformer is using for circuit operation.

Some are resonant converters that must be controlled using varying switching-frequency control, which makes it difficult to optimize their design (especially their magnetic components) as they must be able to operate over a wide range of switching Frequency. Most are voltage-fed, single-stage, pulse width modulation (PWM) converters with a large energy storage capacitor connected across their primary side dc bus. These converters do not have the drawbacks of resonant and current-fed SSPFC converters. They operate with fixed switching frequency, and the bus capacitor

prevents voltage overshoots and ringing from appearing across the dc bus and the 120-Hz ac component from appearing at the output.

Voltage-fed converters, however, have the following drawbacks: The primary-side dc-bus voltage of the converter may become excessive under high input- line and low-output-load conditions. This is because SSPFC converters are implemented with just a single controller to control the output voltage, and the dc-bus voltage left unregulated. The high dc-bus voltage results in the need for higher voltage rated devices and very large bulk capacitors for the dc bus. For example, the converter in has a dc-bus voltage of 600 V. The input power factor of a single-stage voltage-fed converter is not as high as that of current-fed converters. For example, the converter proposed has an input current that is neither continuous nor discontinuous, but is "semi continuous" with a considerable amount of distortion. The converter is made to operate with an output inductor current that is discontinuous for all operation conditions or some parts of operation conditions to try to prevent the dc-bus voltage from becoming excessive output inductor current and dc-bus voltage. Doing so results in the need for components that can handle high peak currents and additional output filtering to remove ripple.

Problems associated with single-stage converters excessive dc-bus voltages due to the lack of a dedicated controller to regulate these voltages, large output ripple, distorted input currents, reduced efficiency (particularly for low input line voltages due to a low dc-bus voltage generally exist for two-level single-stage converters, such as the ones shown in Fig. 1 and three-level converters. In the paper, a new single-stage ac–dc converter that does not have the drawbacks of previously proposed single-stage and two-stage converters is proposed. The paper introduces the new converter, explains its basic operating principles and its modes of operation, and discusses its features and its design. The feasibility of the new converter is confirmed with experimental results obtained from a prototype converter.

The proposed converter has the following features, reduced cost compared to two stage converters, it may expensive, and the reality is that it can be cheaper than a conventional two stage converter. This is because replacing a switch and its associated gate drive circuitry with four diodes reduces cost considerably even though component count seems to be increased this is especially true if the diodes are ordered in bulk numbers. Better performance than a fly back converter, the proposed modified single stage ac-dc converter can operate with a better input power factor for universal input line applications than a single controller, single stage because it does have a dedicated controller for its input section that can perform power factor correction and regulate the dc bus voltage. The presence of second controller also allows the converter to operate with better efficiency and with less output ripple as each section of the converter can be operate in an optimal manner.

It should be noted that although the modified single stage converter with FPGA has the advantages over the conventional two stage converter. As a result, when determining whether to use the modified ac-dc converter versus a fly back two stage converter, the main tradeoffs that needs to be considered is lower cost and improved light-load efficiency versus heavy load efficiency

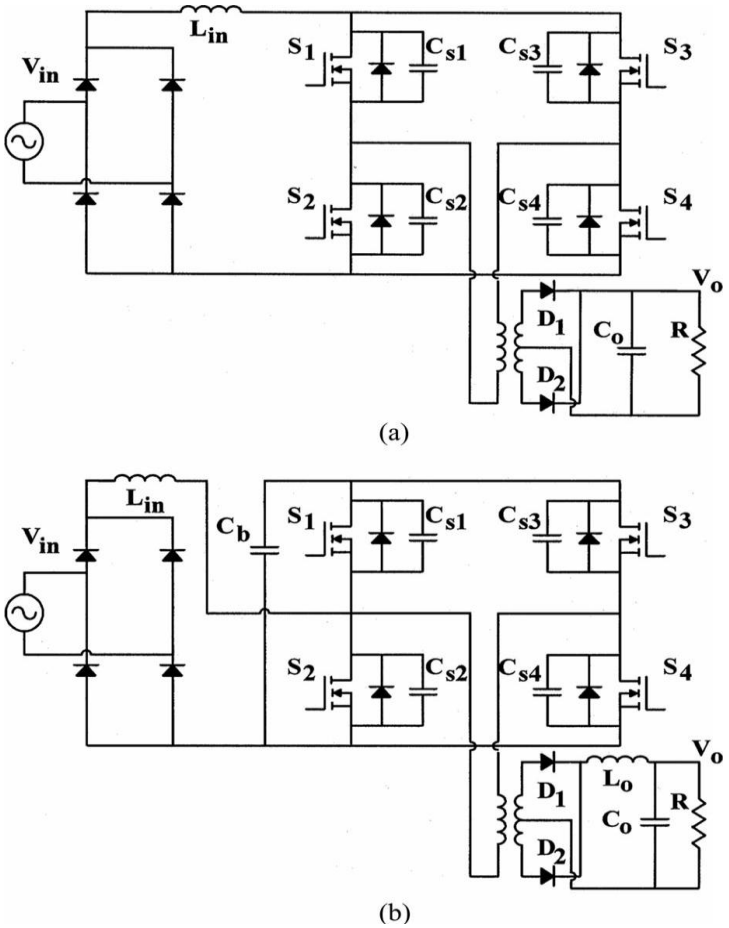

Fig. 1 Varies power factor correction single stage converter. (a) Boost based current fed ac-dc PWM integrated full bridge converter. (b) Power factor correction PWM full bridge converter.

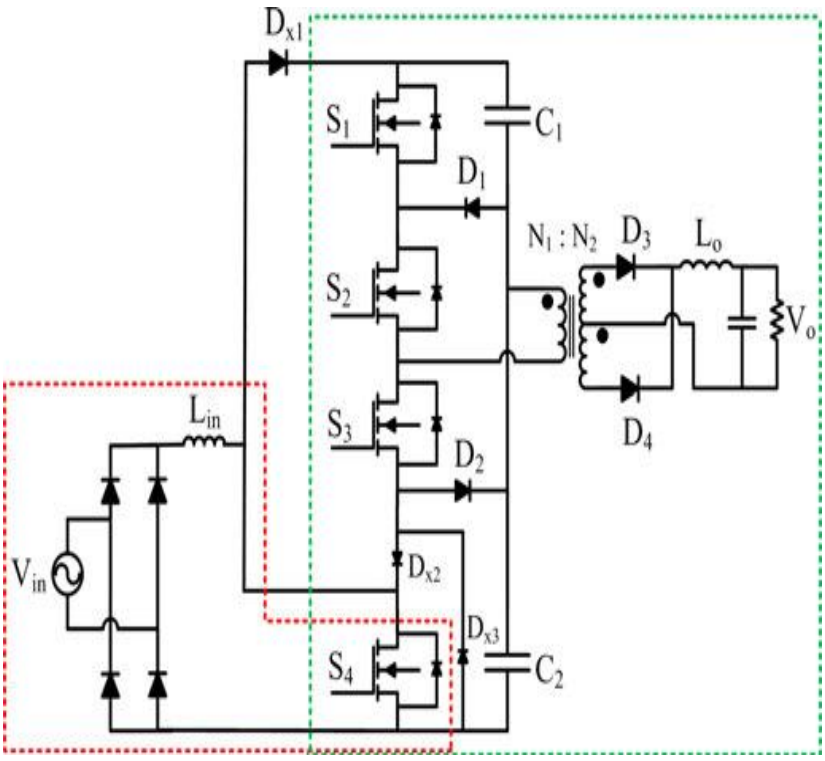

Fig. 2 modified single stage ac-dc converter

II. OPERATION AND WORKING PRINCIPLE

The proposed single stage converter, which is shown in Fig. 2, integrates an ac–dc boost PFC converter into a three-level dc–dc converter. The ac–dc boost section consists of an input diode bridge, boost inductor *L*in, boost diode *Dx*1, and switch *S*4, which is shared by the multilevel dc–dc section. When *S*4 is off, it means that no more energy can be captured by the boost inductor. In this case, diode *Dx*2 prevents input current from flowing to the midpoint of capacitors *C*1 and *C*2 and diode *Dx*1 conducts and helps to transfer the energy stored in the boost inductor *L*in to the dc bus capacitor. Diode *Dx*3 bypasses *Dx*2 and makes a path for circulating current. Although there is only a single converter, it is operated with two independent controllers.

One controller is used to perform PFC and regulate the voltage across the primary side dc-bus capacitors by sending appropriate gating signals to *S*4. The other controller is used to regulate the output voltage by sending appropriate gating signals to *S*1 to *S*4. It should be noted that the control of the input section is decoupled from the control of the dc–dc section and thus can be designed separately. The gating signal of *S*1, however, is dependent on that of *S*4, which is the output of the input controller; how this signal is generated is discussed in detail later in this paper. The gating signals for *S*2 and *S*3 are easier to generate as both switches are each ON for half a switching cycle, but are never ON at the same time. Typical converter waveforms are shown in Fig. 3, and equivalent circuit diagrams that show the converter's modes of operation are shown in Fig. 3 with the diode rectifier bridge output replaced by a rectified sinusoidal source.

As the input line frequency is much lower than the switching frequency, it is assumed that the supply voltage is constant within a switching cycle. It is also assumed that the input current is discontinuous, although there is no reason why the input current cannot be made to be continuous if this is what is desired. The simplified schematic of the power converter and the respective controllers are shown in Fig. 4. The decoupling of the input controller and output controller can occur because the crossover frequencies of the two loops are very different. The crossover frequency of the input controller, which performs input power factor correction and converts input ac into an intermediate dc-bus voltage (voltage across the two primary-side dc-bus capacitors), is much lower than that of the output controller, which converts the intermediate dc-bus voltage into the desired output voltage.

Since the two crossover frequencies are far apart, it is therefore possible to consider the design of one controller to be separate from that of the other. Since the two controllers are decoupled, the standard designs for an ac–dc boost converter controller and a dc–dc full-bridge converter controller can be used. Fig. 4 shows a simple diagram of the controller scheme that has two elements of control. One element is to control dc–dc conversion of the dc-bus voltage to the desired output voltage, and this can be done by controlling the gating signals of *S*1 to *S*4 through controlling duty cycle of *D*1. The other element is to control duty cycle of the switch *S*4 to regulate the dc-bus voltage and to perform input power factor correction. This can be done by controlling *D*2 and then adding duty cycle of *D*2 to *D*1 (where *D*1 and *D*2 are defined in Fig. 3); thus *S*4 performs two tasks; one part (*D*1) participate to control output voltage and another part (*D*2) to regulate dc-bus voltage.

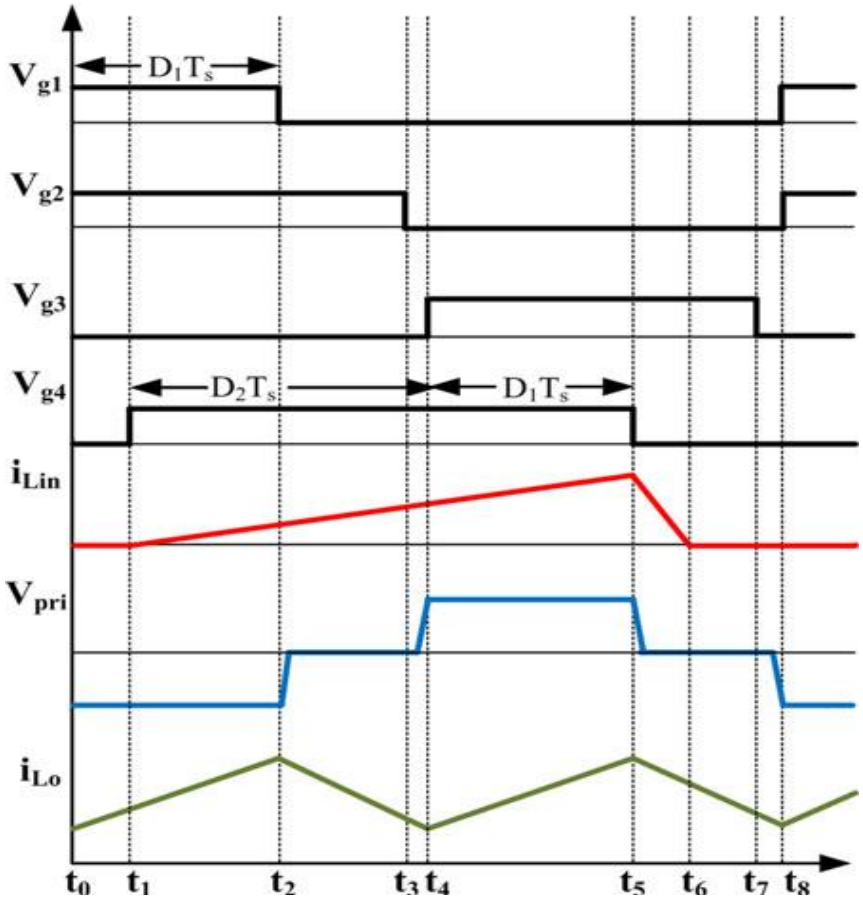

Fig. 3 Typical waveforms describing the switching modes of operation

2.1 DESIGN AND SPECIFICATION OF AC-DC CONVERTER

A procedure for the design of the converter is presented in this section and is demonstrated. The converter is to be designed with the following parameters

1) input voltage: Vin = 90−265 Vrms ;
2) output voltage: Vo = 48 V;
3) maximum output power: Po = 1350 W;
4) switching frequency: fsw=1/TSW = 50 kHz;
5) input current harmonics: IEC1000-3-2 for Class D electrical equipment.

2.2 DETERMINE THE VALUE FOR OUTPUT INDUCTOR (Lo)

The output inductor should be designed so that the output current is made to be continuous under most operating conditions. The minimum value of Lo should be the value of Lo with which the converter's output current will be continuous on the when the converter is operating with maximum input voltage, minimum duty cycle (Dmin), and at least 50% of maximum load. The minimum value of Lo can, therefore, be determined to be

$$L_{o,\min} \geq \frac{V_o^2}{0.5\ P_{o,\max}} \frac{1 - D_m}{2} \frac{T_{\mathrm{SW}}}{2}. \qquad (1)$$

Substituting Po,max = 1350 W, Vo = 48 V, TSW = 20 μs, and Dm = 0.45 gives Lo,min ≥ 9.36 μH and the value of Lo should be larger to provide some margin. It should be noted that such a value is considerably higher than what is typically found in most other single-stage full-bridge converters, which must operate with very low output inductor values to prevent the dc-bus voltage from becoming excessive. A value of Lo = 10 μH, which is just above 9.36 μH, is chosen.

2.3. DETERMINE VALUE FOR TURNS RATIO OF CENTRE TAPPED TRANSFORMER

The relation between Vbus, D, Vo and N is

$$V_o = \frac{V_{\text{bus}}}{2N} D. \qquad (2)$$

The minimum value of N can be found by considering the case when the converter must operate with minimum input line and, thus, minimum primary-side dc-bus voltage Vbus, minimum and maximum duty cycle Dmax. If the converter can produce the required output voltage and can operate with continuous output currents in this case, then it can do so for all cases

$$N \geq \frac{V_{\text{bus,min}}}{2V_o} \cdot D_{\max} \qquad (3)$$

Vbus = 650 V and it is achieved by controlling the S4. Substituting Vo = 48 and Dmax = 0.75, then the value of N should be equal or more than 5. In this example, the value of transformer ratio is considered to be equal to N = 5.

2.4. DETERMINE THE VALUE FOR INPUT INDUCTANCE (Lin)

The value for Lin should be low enough to ensure that the input current is fully discontinuous under all operating conditions, but not so low as to result in excessively high peak current. For the case where Lin is such that the input current remains discontinuous for all operating conditions, the minimum value of Lin determine as

$$L_{\text{in,max}} < \frac{[\![(V_{\text{bus,min}})]\!]^2 * D_{\max} * (1 - D_{\max})^2}{2P_{o,\max} f_{\text{SW}}} \qquad (4)$$

Where,

Dmax = 0.75, Vbus,min = 650 V, Po,max = 1.35 kW, and fSW = 50 kHz. The minimum value of Lin = 114 μH is found. For this design, Lin = 50 mH is used. It should be noted that two controllers can be designed taking into considerations that their crossover frequencies should be wide apart on the s-plane. This is to ensure that the two controllers do not interact with each other. As mentioned earlier, one controller is used to control dc-bus voltage and shape the input current and one controller for control output voltage. The time constant for PFC controller should be faster in compare to output voltage controller

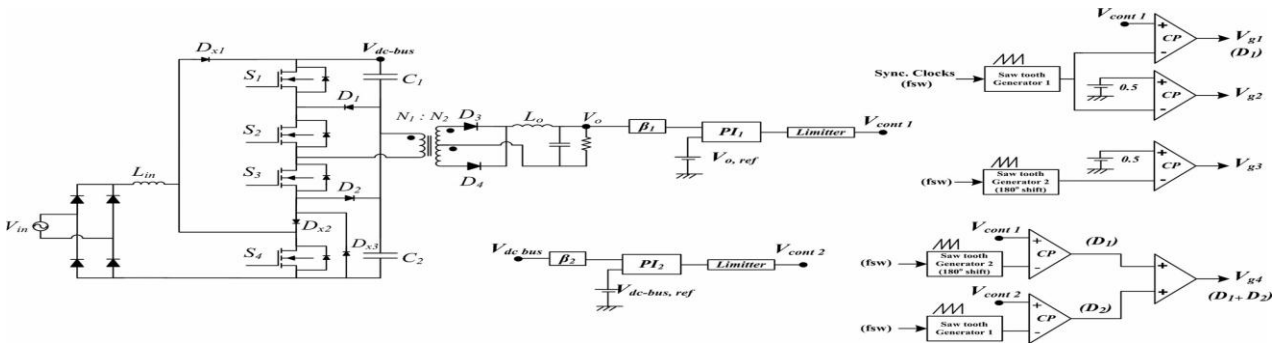

Fig.4. Simplified schematic control of ac-dc converter

III. PWM IMPLEMENTATION WITH FPGA

The PWM strategy is implemented with field programmable gate array. A field programmable gate array is a semiconductor device containing programmable logic components called logic blocks, and programmable interconnects. Logic blocks can be programmed to perform the function of basic logic gates such as AND, and XOR, or more complex combinational functions such as decoders or simple mathematical functions. In most FPGAs, the logic blocks also include memory elements, which may be simple flip-flops or more complete blocks of memory.

A hierarchy of programmable interconnects allows logic blocks to be interconnected as needed by the system designer, somewhat like a one-chip programmable breadboard. Logic blocks and interconnects can be programmed by the customer or designer, after the FPGA is manufactured, to implement any logical function hence the name field-programmable.

FPGAs are usually slower than their application-specific integrated circuit (ASIC) counterparts, cannot handle as complex a design, and draw more power (for any given semiconductor process). But their advantages include a shorter time to market, ability to re-program in the field to fix bugs, and lower non-recurring engineering costs. Vendors can sell cheaper, less flexible versions of their FPGAs which cannot be modified after the design is committed. The designs are developed on regular FPGAs and then migrated into a fixed version that more resembles an ASIC.

3.1 STRUCTURE OF FPGA CONTROLLER

There is only one output, which can be either the registered or the unregistered look up table (LUT) output. The logic block has four inputs for the LUT and a clock input. Since clock signals (and often other high-fan out signals) are normally routed via special-purpose dedicated routing networks in commercial FPGAs, they and other signals are separately managed. Each input is accessible from one side of the logic block, while the output pin can connect to routing wires in both the channel to the right and the channel below the logic block. Each logic block output pin can connect to any of the wiring segments in the channels adjacent to it. Similarly, an I/O pad can connect to any one of the wiring segments in the channel adjacent to it. For example, an I/O pad at the top of the chip can connect to any of the W wires (where W is the channel width) in the horizontal channel immediately below it. Generally, the FPGA routing is unsegmented. That is, each wiring segment spans only one logic block before it terminates in a switch box. By turning on some of the programmable switches within a switch box, longer paths can be constructed. For higher speed interconnect, some FPGA architectures use longer routing lines that span multiple logic blocks.

Whenever a vertical and a horizontal channel intersect, there is a switch box. In this architecture, when a wire enters a switch box, there are three programmable switches that allow it to connect to three other wires in adjacent channel segments. The pattern, or topology, of switches used in this architecture is the planar or domain-based switch box topology. In this switch box topology, a wire in track number one connects only to wires in track number one in adjacent channel segments, wires in track number 2 connect only to other wires in track number 2 and so on. The figure below illustrates the connections in a switch box

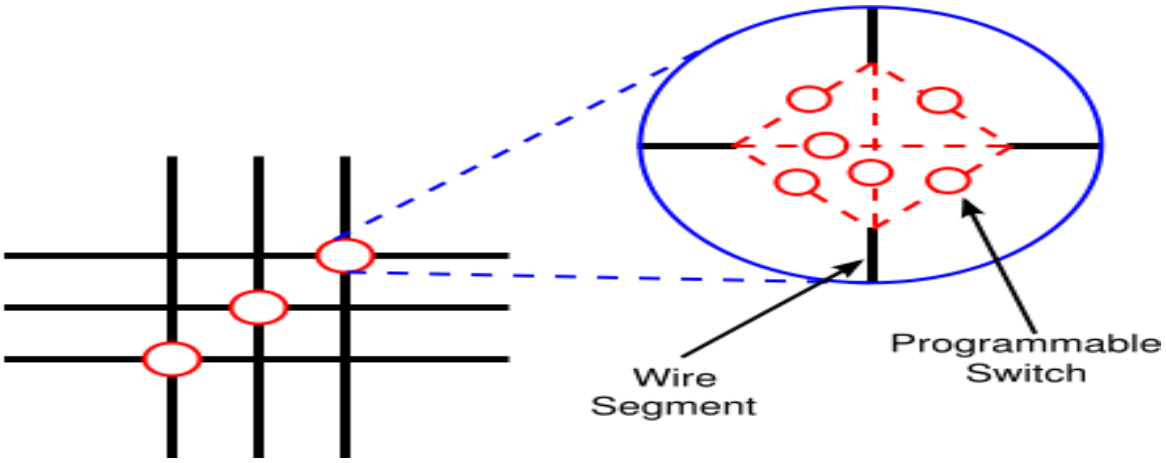

Fig.5. Switch box topology for FPGA controller

Modern FPGA families expand upon the above capabilities to include higher level functionality fixed into the silicon. Having these common functions embedded into the silicon reduces the area required and gives those functions increased speed compared to building them from primitives. Examples of these include multipliers, generic DSP blocks, embedded processors, high speed IO logic and embedded memories.

3.2 DESIGN AND PROGRAMMING FOR FPGA CONTROLLER

To define the behavior of the FPGA the user provides a hardware description language (HDL) or a schematic design. Common HDLs are VHDL and Verilog. Then, using an electronic design automation tool, a technology-mapped net list is generated. The net list can then be fitted to the actual FPGA architecture using a process called place-and-route, usually performed by the FPGA Company's proprietary place-and-route software. The user will validate the map, place and route results via timing analysis, simulation, and other verification methodologies. Once the design and validation process is complete, the binary file generated (also using the FPGA company's proprietary software) is used to (re)configure the FPGA.

In an attempt to reduce the complexity of designing in HDLs, which have been compared to the equivalent of assembly languages, there are moves to raise the abstraction level of the design. Companies such as Cadence, Synopsys and Celoxica are promoting SystemC as a way to combine high level languages with concurrency models to allow faster design cycles for FPGAs than is possible using traditional HDLs. Approaches based on standard C or C++ (with libraries or other extensions allowing parallel programming) are found in the Catapult C tools from Mentor Graphics, and in the Impulse C tools from Impulse Accelerated Technologies. Annapolis Micro Systems, Inc.'s Core Fire Design Suite and National Instruments Lab VIEW FPGA provide a graphical dataflow approach to high-level design entry. Languages such as SystemVerilog, SystemVHDL, and Handel-C (from Celoxica) seek to accomplish the same goal, but are aimed at making existing hardware engineers more productive versus making FPGAs more accessible to existing software engineers. There is more information on C to HDL and Flow to HDL in their respective articles.

To simplify the design of complex systems in FPGAs, there exist libraries of predefined complex functions and circuits that have been tested and optimized to speed up the design process. These predefined circuits are commonly called IP cores, and are available from FPGA vendors and third-party IP suppliers (rarely free and typically released under proprietary licenses). Other predefined circuits are available from developer communities such as Open Cores (typically free, and released under the GPL, BSD or similar license), and other sources.

In a typical design flow, an FPGA application developer will simulate the design at multiple stages throughout the design process. Initially the RTL description in VHDL or Verilog is simulated by creating test benches to simulate the system and observe results. Then, after the synthesis engine has mapped the design to a net list, the net list is translated to a gate level description where simulation is repeated to confirm the synthesis proceeded without errors. Finally the design is laid

out in the FPGA at which point propagation delays can be added and the simulation run again with these values back-annotated onto the net list

3.3. CONSUMED POWER FOR FPGA

FPGA is used to power the logic gates and flip-flops inside the FPGA. The voltage can range from 5V for FPGA generations, to 3.3V, 2.5V, 1.8V, 1.5V and even lower for the latest devices the core voltage is fixed. FPGA requires +3.3V for I/O operations, +2.5V for configuration unit, +1.5V for the core FPGA logic.

IV. SIMULATION AND EXPERIMENTAL RESULTS

4.1. SIMULATION OF MODIFIED SINGLE STAGE AC-DC CONVERTER USING MATLAB/SIMULINK

The simulation results are shown in the figure.9, the simulation digram and the simulation output results separately shown in the figures 8 and 9.

The parameter values is shown below

Vs=100 V,

L=50 mH,

C1 = C2 = 1000e-6 F,

C 3= 220e-6 F

MOSFET = IRF 840

R load = 400 ohms,

Vo =400 V

Centre tapped transformer = 5:1

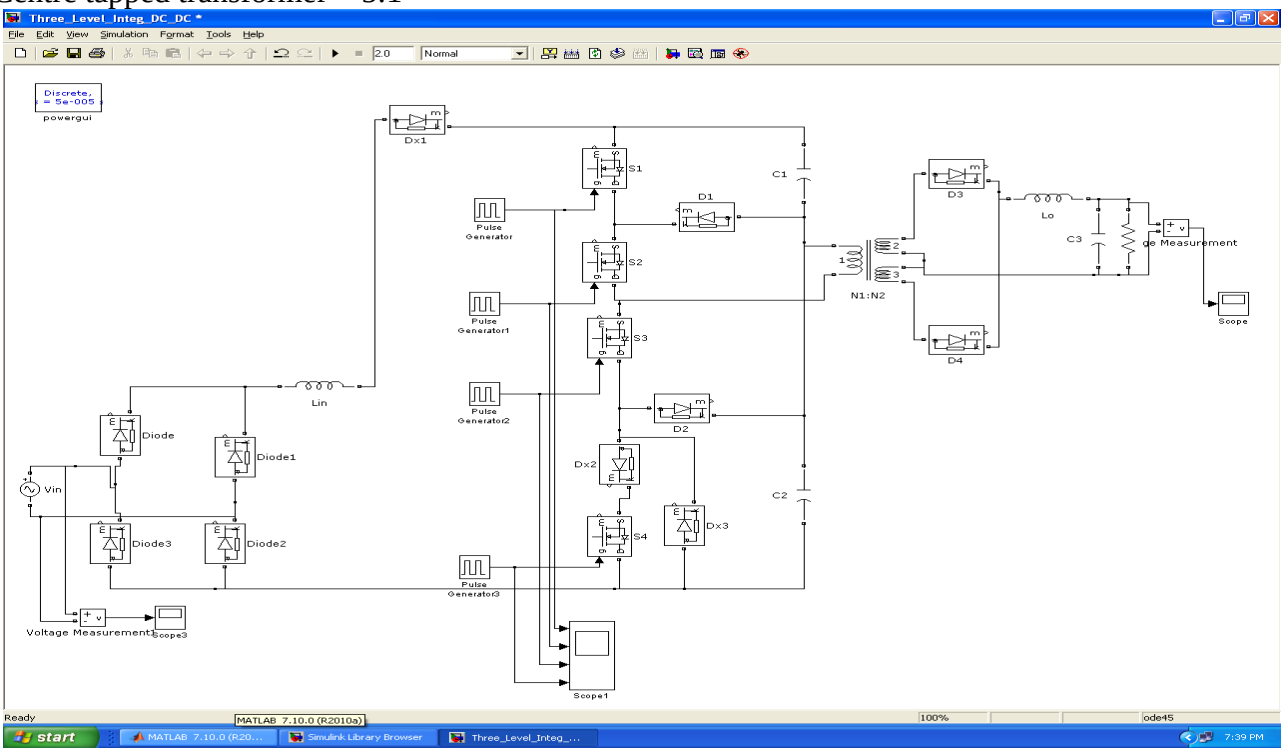

Fig.6 Simulation of modified single stage ac-dc converter using Matlab/Simulink

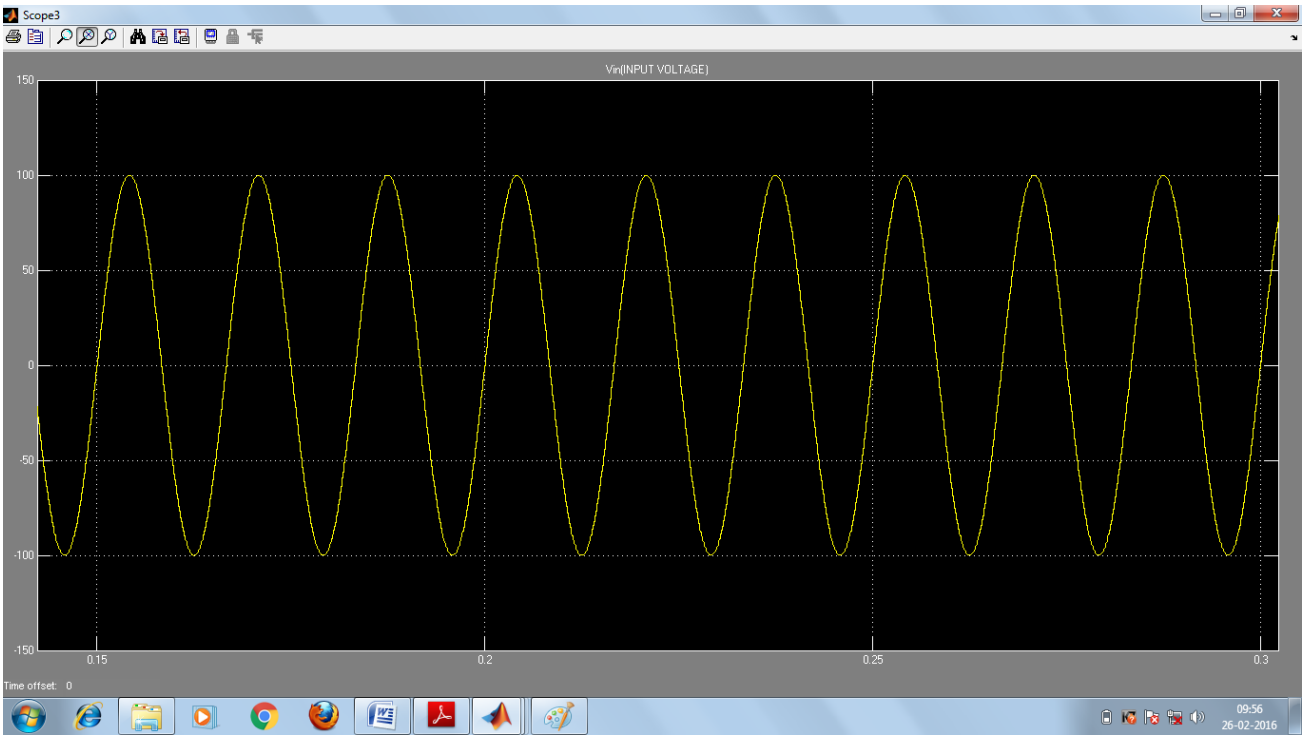

Fig.7 Simulation of input waveform for modified ac-dc converter

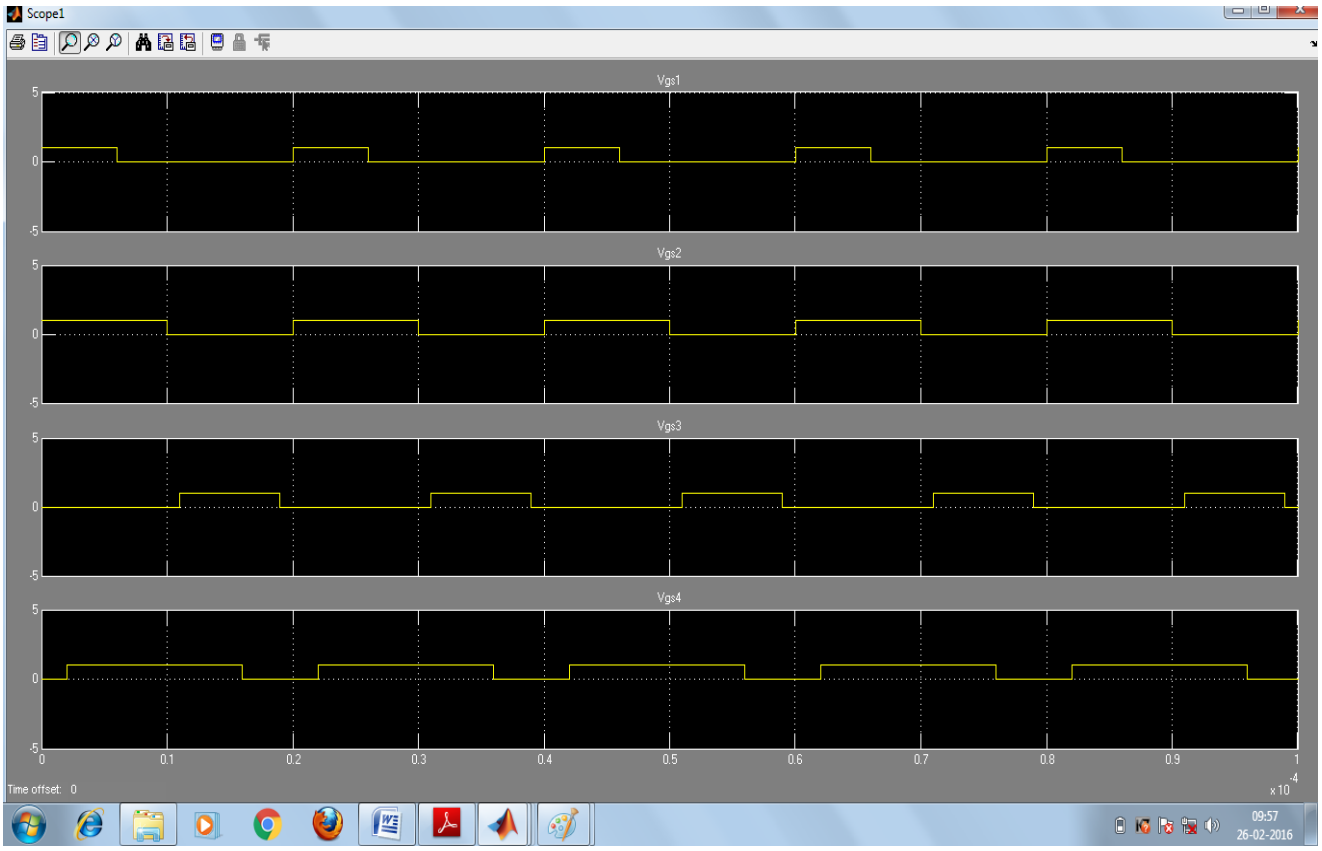

Fig.8 Simulation of switching waveforms for modified ac-dc converter

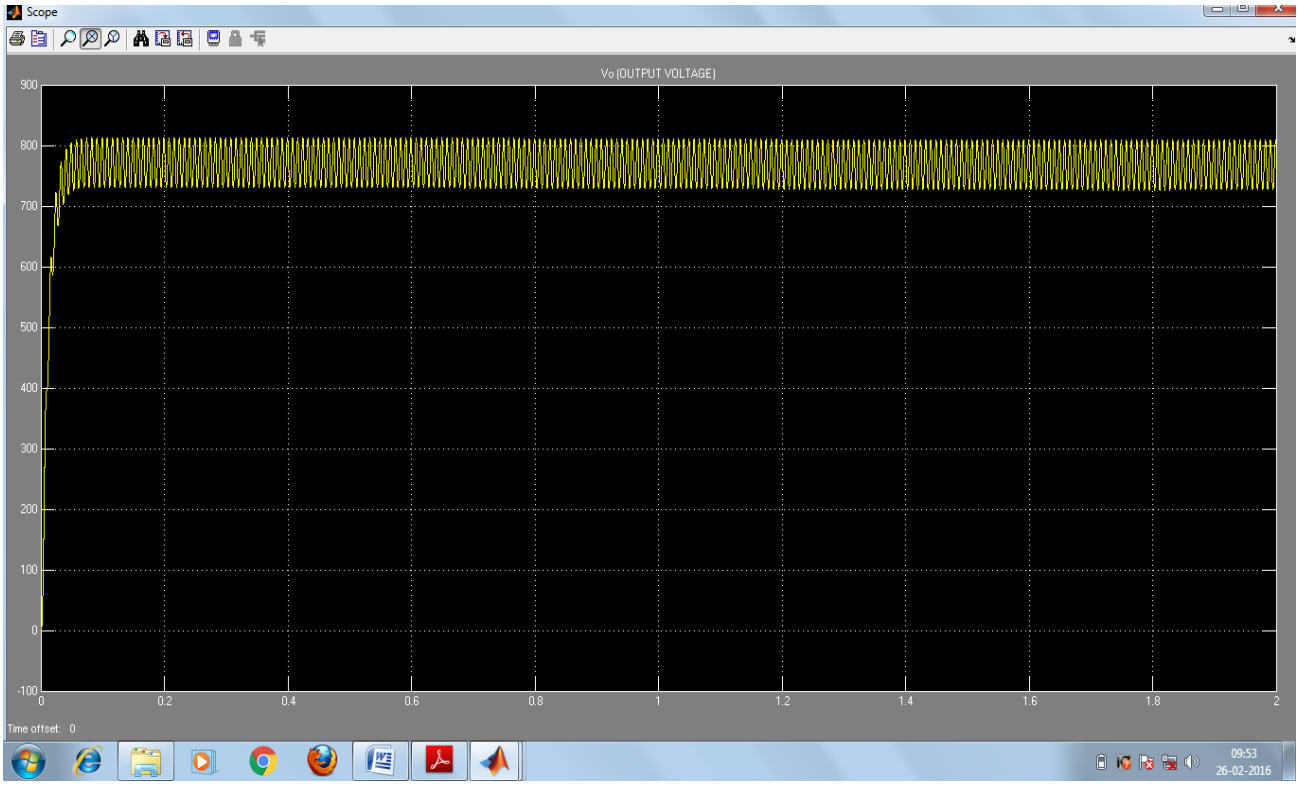

Fig .9 Experimental output voltage V_0

V. CONCLUSION

A modified single stage ac-dc converter using PWM scheme with FPGA controller is proposed in the paper. The outstanding features of this converter are that combines the performance of two stage converters with reduction of cost of single stage converters. This converter is operated with two controller operation with FPGA controller. This converter will be controlled power factor at input and regulated dc voltage at output. The paper introduces the proposed modified single stage ac-dc converter, explains its basic operating principles and PWM operation, and discusses its design with respect to different dc-bus voltages. The operating principle, experimental results of the proposed method have been presented in the paper.

REFERENCES

[1] H. Ma, Y. Ji, and Y. Xu, "Design and analysis of single-stage power factor correction converter with a feedback winding," IEEE Trans. Power Electron., vol. 25, no. 6, pp. 1460–1470, Jun. 2010.
[2] H. S. Athab and D. D.-C. Lu, "A high-efficiency ac/dc converter with quasi-active power factor correction," IEEE Trans. Power Electron., vol. 25, no. 5, p. 1103-1109, May 2010.
[3] J. M. Kwon, W. Y. Choi, and B. H. Kwon, "Single-stage quasi-resonant flyback converter for a cost-effective PDP sustain power module," IEEE Trans. Ind. Electron., vol. 58, no. 6, pp. 2372–2377, Jun. 2011.
[4] H. J. Chiu, Y. K. Lo, H. C. Lee, S. J. Cheng, Y. C. Yan, C. Y. Lin, T. H. Wang, and S. C. Mou, "A single-stage switching flyback converter for power-factor-correction applications," IEEE Trans. Ind. Electron., vol. 57, no.6, pp. 2187–2190, Jun. 2011
[5] H. Athab and D. Lu, "A single-switch ac/dc flyback converter using a CCM/DCM quasi-active power factor correction front-end," IEEE Trans. Ind. Electron., vol. 59, no. 3, pp. 1517–1526, Mar. 2012 J.-Y. Lee, "Single-stage AC/DC converter with inp ut-current dead-zone control for wide input voltage ranges,".IEEE Trans. Ind. Electron., vol. 54,m no. 2, pp. 724–732, Apr. 2007
[6] D. D.-C. Lu, H. H.-C. Iu, and V. Pjevalica, "A single-stage AC/DC converter with high power factor, regulated bus voltage, and output voltage," IEEE Trans. Power Electron., vol. 23, no. 1, pp. 218–228, Jan. 2008.