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# Designing Tunable Subthreshold Logic Circuits Using Adaptive Feedback Equalization

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Abstract—Ultralow-power subthreshold logic circuits are becoming prominent in embedded applications with limited energy budgets. Minimum energy consumption of digital logic circuits can be obtained by operating in the subthreshold regime. However, in this regime process variations can result in up to an order of magnitude variations in ION/IOFF ratios leading to timing errors, which can have a destructive effect on the functionality of the subthreshold circuits. These timing errors become more frequent in scaled technology nodes where process variations are highly prevalent. Therefore, mechanisms to mitigate these timing errors while minimizing the energy consumption are required. In this paper, we propose a tunable adaptive feedback equalizer circuit that can be used with a sequential digital logic to mitigate the process variation effects and reduce the dominant leakage energy component in the subthreshold digital logic circuits. We also present detailed energy-performance models of the adaptive feedback equalizer circuit. As part of the modeling approach, we also develop an analytical methodology to estimate the equivalent resistance of MOSFET devices in subthreshold regime. For a 64-bit adder designed in 130 nm, our proposed approach can reduce the normalized variation of the critical path delay from 16.1% to 11.4% while reducing the energy-delay product by 25.83% at minimum energy supply voltage.

**Keywords**: Feedback equalizer, leakage energy component, subthreshold, variable threshold inverter, Adaptive equalized flip-flop.

## I. INTRODUCTION

The use of subthreshold digital CMOS logic circuits is becoming increasingly popular in energy-constrained applications where high performance is not required. The main idea here is that scaling down the supply voltage can significantly reduce the dynamic energy consumed by digital circuits. Scaling the supply voltage also lowers down the leakage current due to reduction in the drain-induced barrier lowering (DIBL) effect. However, as the supply voltage is scaled below the threshold voltage of the transistors, the propagation delay of the logic gates increases, which in turn increases the leakage energy of the transistors. These two opposite trends in the leakage and the dynamic energy components lead to a minimum energy supply voltage that occurs below the threshold voltage of the transistors for digital logic circuits However, digital logic circuits operating in the subthreshold region suffer from process variations that directly affect the threshold voltage (*VT*). This in turn has a significant impact on the drive current due to the exponential relationship between the drive current and the threshold voltage of the transistors in the subthreshold regime. Moreover, subthreshold digital circuits suffer from the degraded *I*ON/*I*OFF ratios resulting in a failure in providing rail-to-rail output swings when restricted by aggressive timing constraints. These degraded *I*ON/*I*OFF ratios and process-related variations make subthreshold circuits highly susceptible to timing errors that can further lead to complete system failures. Since the standard deviation of *VT* varies inversely with the square root of the channel area , one approach to overcome the process variation is to upsize the transistors. Alternately, one can increase the logic path depth to leverage the statistical averaging of the delay across gates to overcome process variations. These approaches, however, increase the transistor parasitics, which in turn increases the energy consumption. In this paper, we first propose the use of a feedback equalizer circuit for lowering the

energy consumption of digital logic operating in the subthreshold region while achieving robustness equivalent to that provided by. Here, the feedback equalizer circuit (placed just before the flip-flop) adjusts the switching threshold of its inverter based on the output of the flip-flop in the previous cycle to reduce the charging/discharging time of the flip-flop's input capacitance. Moreover, the smaller input capacitance of the feedback equalizer reduces the switching time of the last gate in the combinational logic block. Overall, this reduces the total delay of the sequential logic, which makes it more robust to timing errors and allows aggressive clocking to reduce the dominant leakage energy. In addition to reducing energy consumption, we also demonstrate how the tuning capability of the equalizer can be used to enable extra charging/discharging paths for the flip-flop input capacitance after fabrication to mitigate timing errors resulting from worse than expected process variations in the subthreshold digital logic. In general, our approach of using feedback equalizer to lower energy consumption and improve robustness is independent of the methodology used for designing a combinational logic block operating in the subthreshold regime. The main contributions of this paper are as follows

1) We propose using an adaptive feedback equalizer circuit in the design of tunable subthreshold digital logic circuits. This adaptive feedback equalizer circuit can reduce energy consumption and improve performance of the subthreshold digital logic circuits.

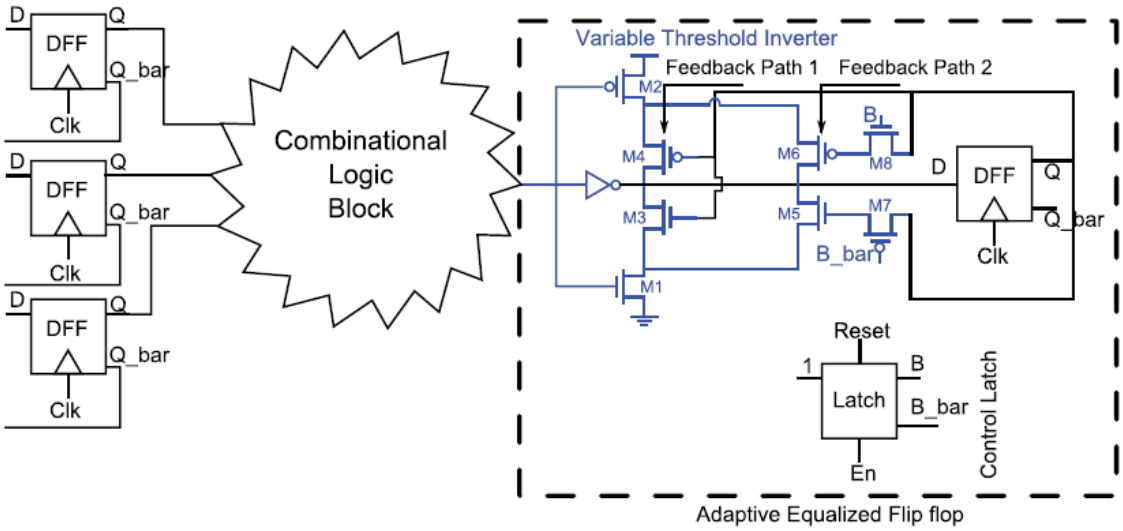
2) We present detailed analytical models (AMs) for performance and energy of the adaptive feedback equalizer circuit. For a 64-bit adder example circuit.

3) We show that compared with , the use of our proposed adaptive feedback equalizer circuit can reduce the energy-delay product (EDP) by 25.83% and also reduce the normalized variation ($3\sigma/\mu$) of the critical path delay from 16.1% to 11.4%.

## II. RELATED WORK

Several techniques have been proposed to design robust ultralow power subthreshold circuits. As described earlier, transistor upsizing [2] and increasing the logic path depth [4], [5] can be used to overcome process variations. The use of gates of different drive strengths has also been proposed to overcome process variations [6]. A detailed analysis on the timing variability and the metastability of the flip-flops designed in the subthreshold region has been presented in [7] and [8], respectively. Lotze and Manoli [9] have used the Schmitt trigger structures in subthreshold logic circuits to improve the *I*ON/*I*OFF ratio and effectively reduce the leakage from the gate output node. Pu *et al.* [10] proposed a design technique that uses a configurable *VT* balancer to mitigate the *VT* mismatch of transistors operating in sbthreshold regime. Zhou *et al.* [11] propose to boost the drain current of the transistors using minimum-sized devices with fingers to mitigate the inverse narrow width effect in subthreshold domain. An analytical framework for subthreshold logic gate sizing based on statistical variations has been proposed in [12], which provides narrower delay distributions compared with the state-of-the-art approaches. Body-biasing has also been proposed to mitigate the impact of variations [13]. A controller that uses a sensor to first quantify the effect of process variations on subthreshold circuits and then generates an appropriate supply voltage to overcome that effect has been proposed in [14]. De Vita and Iannaccone [15] have used a current reference circuit to design a voltage regulator providing a supply voltage that makes the propagation delay of the subthreshold digital circuits almost insensitive to temperature and process variations. Using a differential dynamic logic in standby mode, Liu and Rabaey [16] propose to suppress leakage in the subthreshold circuits. Error detection and correction techniques have been widely used to design resilient, energy-efficient above threshold architectures [17]–[20]. Tschanz *et al.* [17] and Bowman and Tschanz [18] have used a tunable replica circuit (with 3.5% leakage power overhead, 2.2% area overhead), and error-detection sequentials (with 5.1% leakage power overhead and 3.8% area overhead) to monitor critical path delays and mitigate dynamic variation guardbands for maximum throughput in the above-threshold regime.

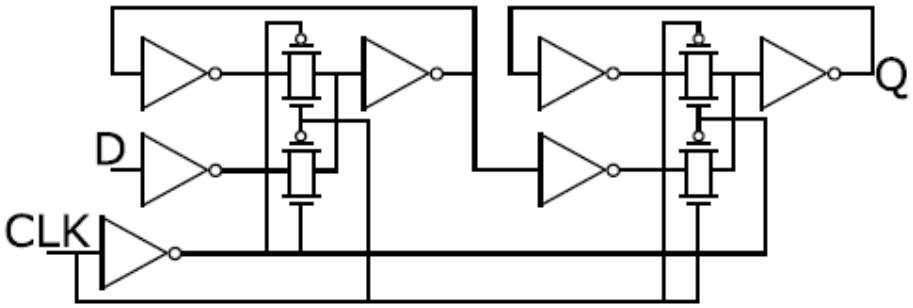



*"Figure 1. Adaptive feedback equalizer circuit with multiple feedback paths (designed using a variable threshold inverter can be combined with a traditional master–slave flip-flop to design an adaptive E-flip-flop".*

## III. ADAPTIVE EQUALIZED FLIP-FLOP VERSUS CONVENTIONAL FLIP-FLOP

In this section, we first explain the use of the adaptive feedback equalizer circuit in the design of an adaptive equalized flip-flop (E-flip-flop) and then provide a detailed comparison of the E-flip-flop with the conventional flip-flop in terms of area, setup time, and performance. We propose the use of a variable threshold inverter as an adaptive feedback equalizer along with the classic master–slave positive edge-triggered flip-flop design an adaptive E-flip-flop. This adaptive feedback equalizer circuit consists of two feedforward transistors (M1 and M2 in Fig. 1) and four control transistors (M3 and M4 for feedback path 1 that is always ON and M5 and M6 for feedback path 2 that can be conditionally switched ON postfabrication in Fig. 1) that provide extra pull-up/pull-down paths in addition to the pull-up/pull-down path in the static inverter for the Data Flip- Flop input capacitance. The extra pull-up/pull-down paths are enabled whenever the output of the critical path in the combinational logic changes. The control transistors M5 and M6 are enabled/disabled through transistor switches (M7 and M8) that are controlled by an asynchronous control latch. The value of the static control latch is initially reset to 0 during chip bootup. After bootup, if required a square pulse is sent to the En terminal to set the output of the latch to 1 to switch ON M7 and M8, which enables feedback path 2.

The adaptive E-flip-flop effectively modifies the switching threshold of the static inverter in the feedback equalizer based on the output of flip-flop in the previous cycle. If the previous output of the flip-flop is a 0, the switching threshold of the static inverter is lowered, which speeds up the transition of the flip-flop input from 0 to 1. Similarly if the previous output is 1, the switching threshold is increased, which speeds up the transition to 0. Effectively, the circuit adjusts the switching threshold and facilitates faster high-to-low and low-to-high transitions of the flip-flop input. Moreover, the smaller input capacitance of the feedback equalizer reduces the switching time of the last gate in the combinational logic block. Overall, this reduces the total delay of the sequential logic. The dc response of the adaptive feedback equalizer circuit with two different feedback paths in the subthreshold regime is shown in Fig. 3. The adaptive E-flip-flop has eight more transistors than the conventional master–slave flip-flop . Compared with a classic master–slave flip-flop with 22 transistors ,the area overhead of the adaptive E-flip-flop is 36%.




*"Figure 2. Circuit diagram of classic master–slave positive edge-triggered flip-flop".*

control latch with ten transistors (three inverters and two TGs) is 45%. This area overhead gets amortized across the entire sequential logic block. The total energy consumed by a digital circuit in the subthreshold regime can be calculated using

$$ET = EDYN + EL = CeffV\,2DD + IleakVDDTD. \quad (1)$$

In (1), *E*DYN and *EL* are the dynamic and leakage energy components, respectively. *C*eff is the total capacitance of the entire circuit, *V*DD is the supply voltage, and *TD* = 1*/f* is the total delay along the path of the digital logic block. Feedback equalization enables us to reduce the delay of the path in the digital logic block, which in turn reduces the leakage energy. In (1), *I*leak is the leakage current and can be written as

$$Ileak = \mu 0 Cox WL(n-1)V2\ the\ \eta VDS - VT\ nVth\ . \quad (2)$$

In (2), *VT* is the transistor threshold voltage, *V*th is the thermal voltage, *n* is the subthreshold slope factor, and $\eta$ is the DIBL coefficient. There is an exponential relationship between the leakage current and the supply voltage (due to the DIBL effect and because *V*DS ≈ *V*DD). Using the E-flip-flop, we can scale down the supply voltage while maintaining the zero-error rate at a given operating frequency and achieve lower dynamic energy consumption (due to the quadratic relationship between the dynamic energy and the supply voltage) as well as lower leakage energy (due to smaller DIBL effect that exponentially decreases the leakage current). Similar to the area overhead, the dynamic energy as well as the leakage energy overhead of the variable threshold inverter gets amortized across the entire sequential logic block. The setup time of the conventional master–slave positive edge-triggered flip-flop is *ts*−*t* = 3*t*inv + *t*TG. Since the adaptive E-flip-flop uses an extra variable-threshold inverter at its input, the setup time of the adaptive E-flip-flop will be larger *ts*−*t*−equ ≈ 4*t*inv + *t*TG. The clk-to-*q* delay of the conventional flip-flop is *tc*−*q* = *t*inv + *t*TG. Since the E-flip-flop has the variable threshold inverter as extra load at the output, the *tc*−*q* delay of the E-flip-flop is *tc*−*q*−equ = *t*inv+*t*TG +_*tc*−*q* , which is slightly larger than the *tc*−*q* delay of the conventional flip-flop. Here, _*tc*−*q* is the increase in inverter delay due to the extra load of the adaptive feedback equalizer circuit. However, the adaptive feedback equalizer circuit can significantly lower down the propagation delay of the critical path because the small input capacitance of the feedback equalizer reduces the switching time of the last gate in the combinational logic. The hold time of the classic master–slave positive edge-triggered flip-flop is zero. Therefore, the adaptive feedback equalizer circuit does not impact the hold time violations. Table I compares the propagation delay, setup time, and the *tc*−*q* delay of the two 64- bit adders designed with the conventional flip-flop and E-flipflop in United Microelectronics Corporation (UMC) 130-nm process when operating with different supply voltages in the subthreshold regime.

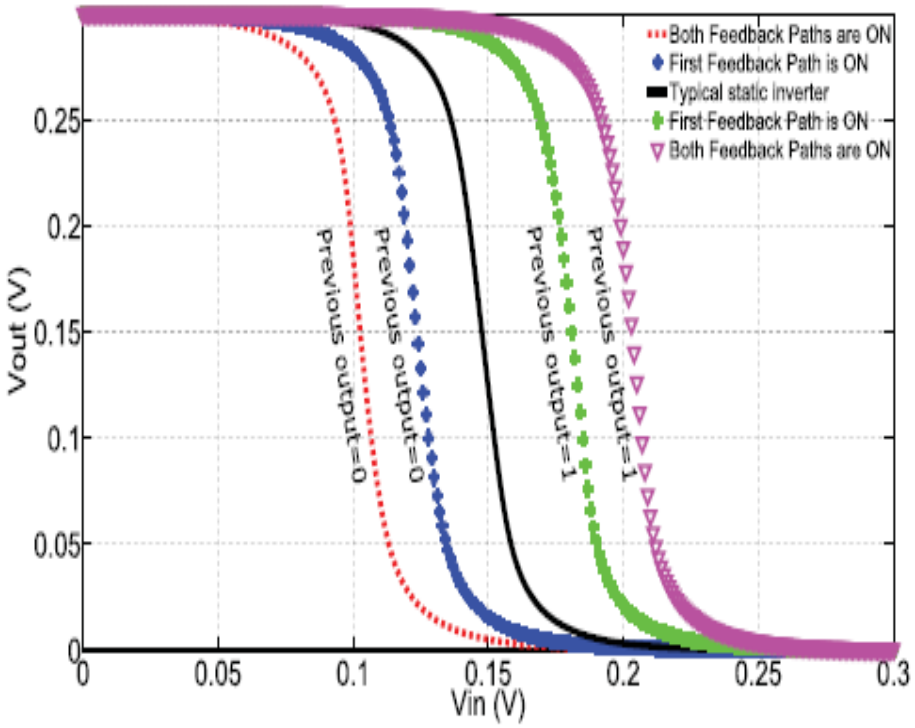



***Figure 3. DC response of the adaptive feedback equalizer circuit with two different feedback paths***

***Table 1. Comparison between the timing characteristics of the e-logic design with the conventional ne-logic design of 64-bit ader***

| Supply voltage (mV) | Propagation delay NE-logic (ns) | Propagation delay E-logic (ns) | $t_{c-q}$ NE-flip flop (ns) | $t_{c-q-eq}$ E-flip flop (ns) | $t_{s-t}$ NE-flip flop (ns) | $t_{s-t-eq}$ E-flip flop (ns) |
|---|---|---|---|---|---|---|
| 350 | 35 | 27 | 3.82 | 4.06 | 6.07 | 8.70 |
| 330 | 49 | 38 | 5.66 | 6.51 | 9.01 | 13.51 |
| 310 | 70 | 58 | 8.23 | 10.90 | 13.11 | 19.74 |
| 290 | 107 | 80 | 12.61 | 16.71 | 20.09 | 30.25 |
| 270 | 150 | 117 | 17.87 | 23.67 | 28.49 | 42.73 |
| 250 | 248 | 210 | 27.89 | 36.95 | 44.46 | 66.69 |

Moreover, the switching threshold of the adaptive feedback equalizer circuit should still be larger than the amplitude of the glitch. This would specify the maximum allowable feedback strength of the adaptive feedback equalization technique (maximum tolerable glitch amplitude. The sampling of a glitch leads to the marginal increase in the dynamic energy of the sequential logic block (0.72% increase in the 64-bit adder), but it has a negligible impact on the overall energy consumption as it is not the dominant energy component in the subthreshold regime. The feedback equalizer circuit also reduces the pulse width of the glitch (by 41%).

This decreases the required guardband in the clock period to avoid sampling the glitch (and hence we can reduce the clock period), which ultimately reduces the dominant leakage energy component of the subthreshold logic block by 5.1% in the 64-bit adder at minimum-energy supply

voltage. To avoid the metastability problem in the E-flip-flop, both the setup time and holdtime constraints should be satisfied.

The setup time and the clk-to-*q* delay of the adaptive E-flip-flop are larger than that of the classic master–slave positive edge-triggered flip-flop. However, the feedback equalizer circuit can lower down the propagation delay of the critical path since it significantly reduces the switching time of the last gate in the combinational logic. Therefore, if we match the clock period for both the NE-logic and the E-logic, then the setup time condition is easily met. In fact, it should be noted that the E-logic enables a reduction in the clock period (Table I). The hold time constraint of the flip-flop is as follows:

where *t*cdFF is the minimum propagation delay of the flip-flop and *t*cdlogic is the minimum propagation delay of logic.The hold time of the E-flip-flop is zero. So, the hold time constraint is also fulfilled, which insures the stability of feedback equalizer circuit in the subthreshold regime.

$$t\text{hold} < t\text{cdFF} + t\text{cdlogic} \quad (3)$$

the dominant leakage energy component of the subthreshold logic block by 5.1% in the 64-bit adder at minimum-energy supply voltage. To avoid the metastability problem in the E-flip-flop, both the setup time and holdtime constraints should be satisfied.

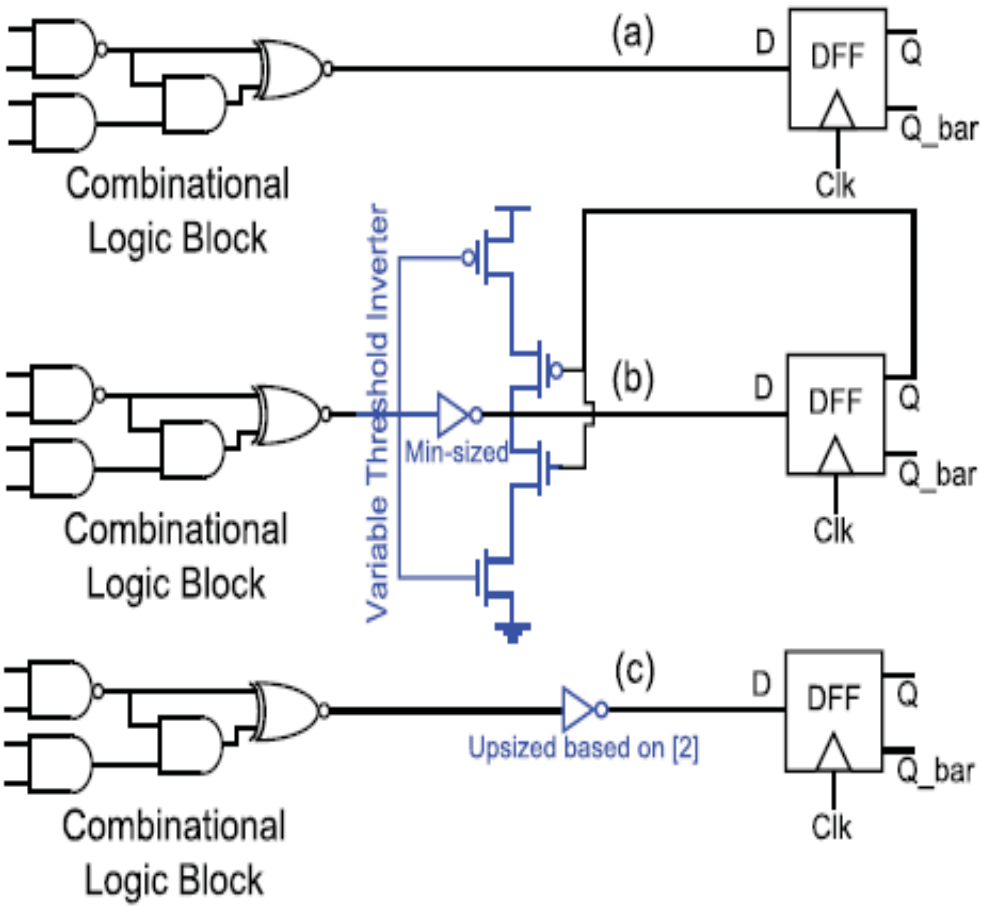



***Figure 4. Block diagrams of (a) original nonequalized design, (b) equalized design with one***

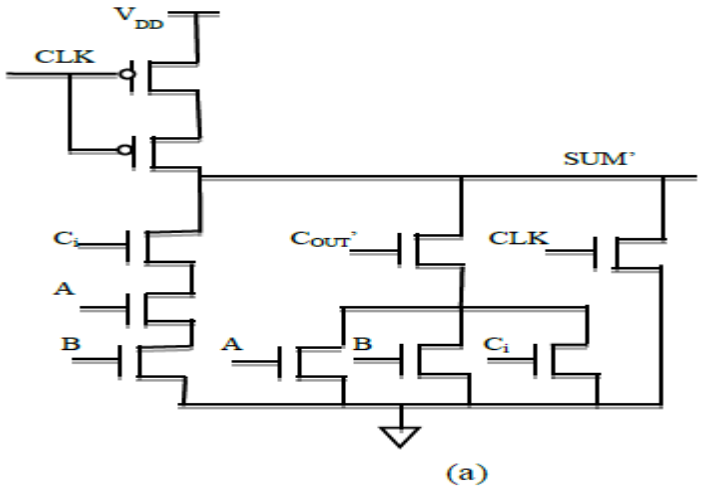
*feedback path ON, (c) buffer-inserted nonequalized design.*

*Table 2. Comparison between the timing characteristics of the e-logic design with the conventional ne-logic design of 64-bit ader*

| Technology Node (nm) | Logic Style | Min-Energy Supply Voltage (mV) | Leakage Energy (fJ/cycle) | Dynamic Energy (fJ/cycle) | Delay (ns) |
|---|---|---|---|---|---|
| 45 | NE-logic | 287 | 11 | 9 | 52 |
| 45 | E-logic | 287 | 8.5 | 10.1 | 40.1 |
| 65 | NE-logic | 290 | 11.9 | 12.9 | 56.1 |
| 65 | E-logic | 290 | 9.5 | 14.1 | 43.9 |
| 90 | NE-logic | 295 | 15 | 18.9 | 61 |
| 90 | E-logic | 295 | 12.4 | 20 | 50 |
| 130 | NE-logic | 300 | 21.1 | 28.9 | 69.5 |
| 130 | E-logic | 300 | 17.9 | 30.1 | 59.1 |

## IV. PERFORMACE ANALYSIS OF PROPOSED MODIFIED FTL

The two proposed modified FTL structure's performance is verified against the existing FTL structure by designing a long chain of inverter consisting 10 stages. We have used 0.18µm CMOS process technology model library from UMC, using the parameter for typical process corner at 25 0C. Power supply VDD is constant for all simulations and is equal to 1.8V. Circuits are simulated in HSPICE simulator. show the plot of output voltage from the 1st stage of inverter to the 10th stage of inverter at 20 fF capacitive loads for existing FTL, proposed modified LP-FTL and HS-FTL respectively. the VOL value of LP-FTL is less than that of existing FTL . The transition for HS-FTL occurs from VTH to either VOH or VOL 20 fF capacitive load at 100 MHz. The LP-FTL structure provides reduction in power consumption due to reduction in VOL. The power consumption by LP-FTL structure is 36.8% less than that of FTL in [7].The HS-FTL structure provides improvement in average propagation delay by a factor of 1.83 with respect to LP-FTL and 1.36 with respect to FTL. The power delay product of both the proposed modified FTL structure is better as compared to existing FTL structure.




(a)

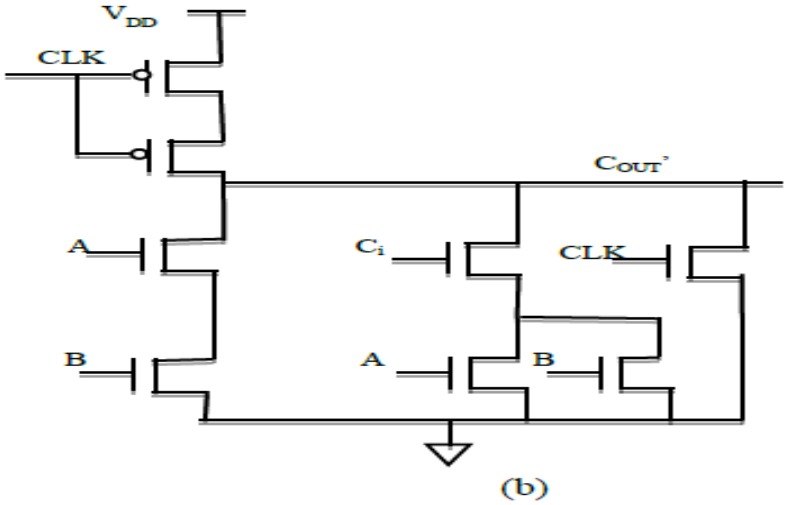



*Figure 5. LP-FTL structure of (a) sum cell (b)carry cell.*

## V. RIPPLE CARRY ADDER DESIGN AND PERFORMANCE ANALYSIS

A full adder is designed by using these basic sum and carry cell shown in Fig. 5(a), (b). These basic cells are designed by using proposed modified LP-FTL structure. These cells are used for the design of 8-bit ripple carry adder as in [4]. Cells for the HS-FTL structure are similar. All the 8-bit ripple carry adders designed by various structures are simulated in 0.18μm CMOS process technology model library from UMC, using the parameter for typical process corner at 250C. Power supply VDD is constant for all simulations and is equal to 1.8V. Dynamic power consumption, propagation delay time (tp), and power delay product (PDP) of existing FTL structure in [7], LP-FTL and HS-FTL structure for 10 fF capacitive loads at 100 MHz. With respect to the existing FTL structure the proposed LP-FTL structure provides 38% reduction in dynamic power. The proposed HS-FTL structure achieves a speed up factor of 2.65 with respect to LP-FTL structure and 1.96 with respect to existing FTL structure the PDP chart the PDP of both the proposed structures are better as compared to the existing FTL structure. The PDP improves due to reduction in power in LP-FTL and reduction in average propagation delay in HS-FTL structure. are the plots of propagation delay versus load capacitance (variation from 1 fF to 20 fF) and temperature (variation from -20 0C to 120 0C). The effect of inter-stage load capacitance on dynamic power is shown in Fig. 8. by varying load capacitance from 1 fF to 20 fF. The power consumption of the proposed LP-FTL structure is less as compared to the other structures.

***Table 3 . Simulation results for dynamic power for an 8-bit ripple carry adder designed by proposed ftl circuits and the existing ftl structure***

| Logic family | Power(μW) | $t_p$(ns) | PDP (μW*ns) |
|---|---|---|---|
| FTL in [7] | 409.68 | 0.63 | 258.09 |
| Proposed LP-FTL | 249.91 | 0.85 | 212.42 |
| Proposed HS-FTL | 540.12 | 0.32 | 172.83 |

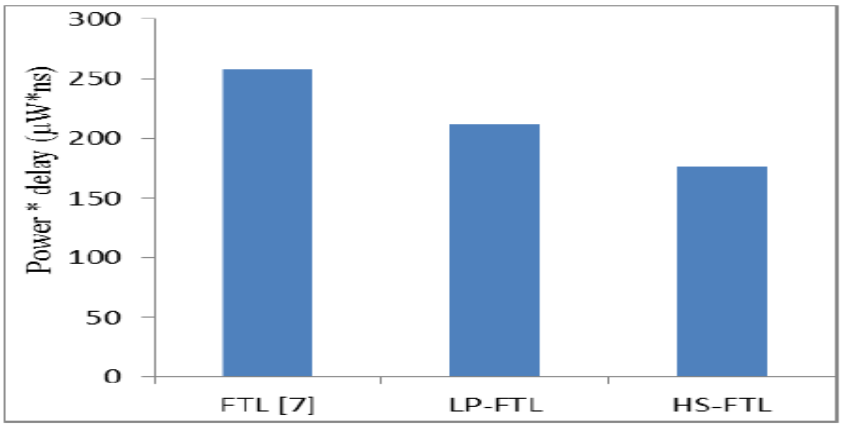



*Figure 6. Power delay product for RCA*

## VI .CONCLUSION

In this paper we proposed a low power dynamic circuit. The proposed circuit is simulated in 0.18 µm CMOS process technology from UMC. The proposed modified circuit when compared with the recently proposed scheme the LP-FTL structure reduces dynamic power consumption by at-least 35% as compared to existing FTL structure and the HS-FTL structure provides a speed up factor of at-least 1.35 over the LP-FTL and existing FTL structure. The simulation for a long chain of inverter (10-stage) and 8-bit ripple carry adder is also carried out in this work. The simulation result confirms that for a given load and at same frequency of operation the power delay product of both the proposed circuits is much better than that of existing FTL structure.

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