Scientific Journal Impact Factor (SJIF) : 1.711
International Journal of Modern Trends in Engineering and Research
ISSN (ONLINE) : 2349 - 9745
ISSN (PRINT) : 2393 - 8161

SPACE VECTOR MODULATION FOR NINE-SWITCH INVERTER

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Abstract— This paper proposes space vector modulation for nine switch inverter as dual output inverter. proposed technique compared with carrier based PWM technique and space vector modulation technique (SVM).SVM technique increases the sum modulation indices up to 15% in contrast with conventional scheme, in which the sum of modulation indices is equal or less than one. The extra high voltage available for a given input dc-voltage translates to higher torque. This paper introduces novel SVM technique with minimum semiconductor switching and reduced THD .Min semiconductor switching method reduces the cost of power devices and thermal heat effect ,this scheme will be advantages for high power applications .Where as reduce THD method minimize the total harmonic distortion .The performance of proposed SVM for nine switch inverter is verified by simulation .

Keywords— Nine –switch inverter , Space Vector Modulation (SVM),SPWM.

I. INTRODUCTION

Inverters are used as dc/ac converter and power controller for ac load such as motor drivers. In many cases, there are two or more ac loads, which require independent control. The conventional solution is to use separate inverters. This increases cost and volume of system. A dual output inverter has been presented in [1] using only nine semiconductor switches (see Fig. 1). This inverter is known as nine- switch inverter and is also used as an ac/ac converter in [2] and [3]. The nine-switch inverter is composed of two conventional inverters with three common switches .in nine-switch inverter sum modulation index of two outputs must be less than or equal to one. Therefore, voltage amplitude of outputs is smaller, compared with two separate inverters [4].This problem can rectify by space vector modulation. In [1], carrier-based pulse width modulation (PWM) methods have been proposed for nine-switch inverter. This paper proposes space vector modulation (SVM) methods for the aforementioned nine-switch inverter .This paper is organized as follows. Section II describes the carrier-based PWM control method for nine-switch inverter. Section III describes the proposed SVM for nine-switch inverter, as well as two special SVMs with minimum switching number and THD. Section IV presents simulation and experimental results.

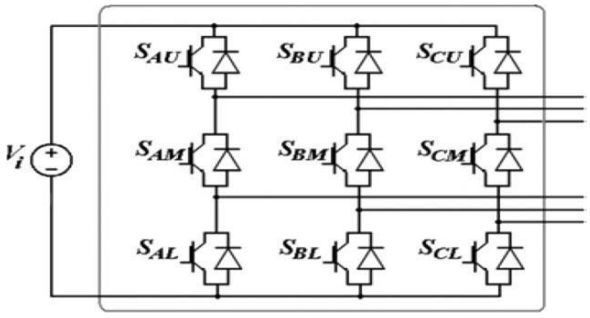

Figure 1. Nine-switch Inverter

II. CARRIER BASED PWM METHOD

The carrier-based PWM control method for nine- switch inverter is shown in Figure. 2. There are two reference signals (upper and lower) for each phase. The upper and lower reference signals are related to upper and lower outputs respectively. The gate signal for upper switch of leg generated by comparing the carrier signal and upper reference signal of the related phase ($VrefU\ J$). Similarly, the gate signal for lower switch is generated from the carrier signal and lower reference signal of the related phase ($VrefL\ J$). The gate signal for mid switch is generated by the logical XOR of the gate signals for upper and lower switches. With this method, always two switches are ON in each leg.

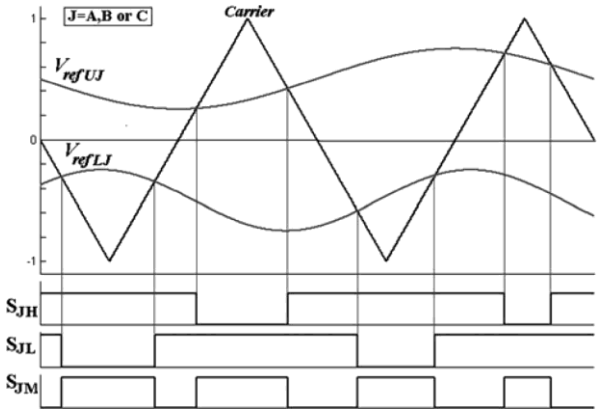

Figure 2. Carrier-based PWM method switching inverter

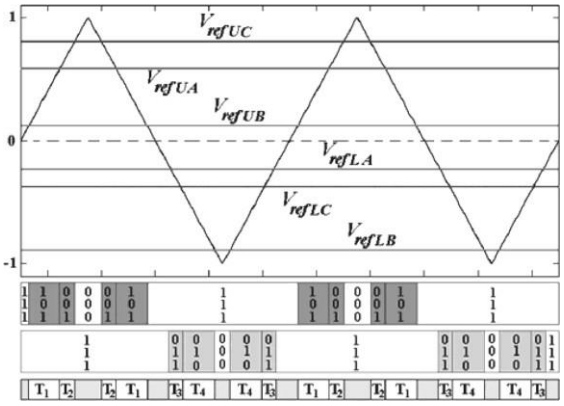

Figure 3. Carrier-based PWM method switching vector

Figure 3. shows carrier-based PWM method switching vectors. There are six vectors in each switching cycle for both outputs: two nonzero vectors, one zero vector 0 0 0, two none zero vectors and one zero vector 1 1 1 *{*two active—short zero (0 0 0)—two active—long zero (1 1 1)*}*. In an active vector, output load is connected to the dc input source, while in a zero vector, the output load is short-circuited.

III. SVM FOR NINE-SWITCH INVERTER

In regard to Figure. 2, each leg can be in three different semiconductors ON-OFF position. These position can be called *{*1*}*, *{*0*}*, and *{*−1*}*, as is illustrated in Table I. In Table I, *J* refers to leg *A*, *B*, or *C* and *U*, *M*, *L* refers to upper, mid, and lower semiconductors respectively. The combination of switching vector of both outputs in Figure 3 specific sequence as shown in Fig. 4. This sequence is used to design SVM method. There are 12 vectors in each switching cycle: *{*two upper active (V_{AU})— zero (V_Z)—two upper active (V_{AU})—zero (V_Z)—two lower active (V_{AL})—zero (V_Z)—two lower active (V_{AL})—zero (V_Z)*}*. The switching vectors are listed in Table II. The vectors *V*1–*V*6 are upper active vectors. In these vectors, the upper output is in active state, and the lower output is in zero state. There is an inverse logic in lower active vectors (*V*7–*V*12). In zero vectors (*V*13–*V*15), both outputs are in zero state.

	S_{JU}	S_{JL}	S_{JM}
1	ON	OFF	ON
0	OFF	ON	ON
-1	ON	ON	OFF

Table 1. Semiconductors on-off position of leg

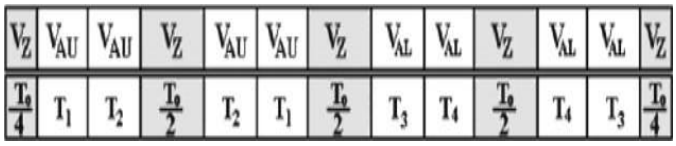

Figure 4. Typical SVM switching vector sequence

Table 2. SVM switching vectors

Vector	Leg A	Leg B	Leg C	Type
1	1	0		
2	0			
3	1	1		
4	0			Upper Active
5	0	1		
6	-1	1		
7	1			
8	-1	-1		
9	1			
10	1	-1		Lower
11	1	1		
12	1			Zero
13	0	0		
14	0			
15				

Table II does not include all possible variations of switching states *{1}*, *{0}*, and *{−1}*. Since a vector including *{−1}* and *{0}* connects both loads to the dc source at the same time, the loads lose their independence and they cannot have independent frequencies. This is the reason for avoiding a vector that includes combinations of *{−1}* and *{0}*.To determine the proper active vectors, two space vector diagrams are proposed as shown in Fig. 5. The diagrams (a) and (b) are used to determine the upper and lower active vectors, respectively. The SVM active vectors are determined with regard to location of upper reference signal (vrefU)in the diagram(a) and lower refernce signal(vrefL) in the diagram (b). The reference signals for the upper and lower outputs are defined as,

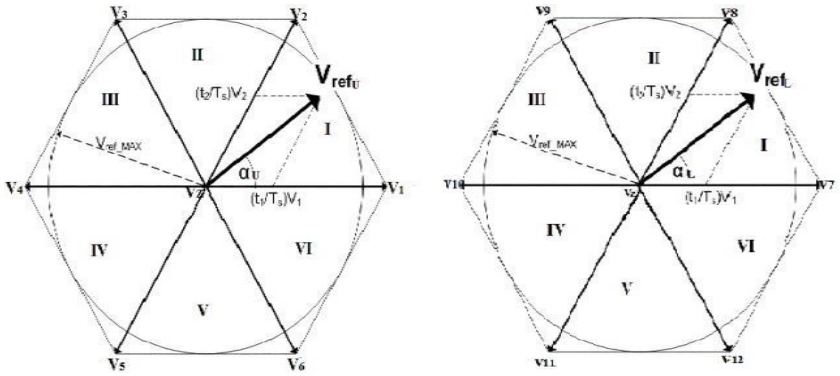

Figure 5. Space vector diagrams for nine-switch inverter.(a) Upper output (b) Lower output

$$\bar{V}refL = VrefL \angle \alpha_L$$

where

$$\alpha U = 2\pi f Ut + \emptyset U$$
$$\alpha L = 2\pi f Lt + \emptyset L$$

where fU ,fL are the frequencies, and $\emptyset U, \emptyset L$ are the phases. All zero vectors V_{13},V,V can be used for zero states. The type of zero vectors can be selected based on control goals and optimizations such as minimum number of semiconductor switchings.

The switching time intervals of vectors are calculated as

$$T1 = \frac{\sqrt{3}}{2} mUTsin(\frac{\pi}{3} - \alpha U)$$
$$T2 = \frac{\sqrt{3}}{2} mUTsin(\alpha U)$$
$$T3 = \frac{\sqrt{3}}{2} mLTsin(\frac{\pi}{3} - \alpha L)$$
$$T4 = \frac{\sqrt{3}}{2} mLTsin(\alpha L)$$

where $T1$, $T2$ are the time interval of upper active vectors, $T3$, $T4$ are time of lower active vectors, To is time of zero vectors and T is switching period. U and L are upper and lower modulation indices, respectively, and defined by

$$mU = 2\frac{VrefU}{Vi}$$
$$mL = 2\frac{VrefL}{Vi}$$

The sum of active vector time intervals must be less or equals to T. Thus, the following constrain must be satisfied .

$$(mU + mL) \leq \frac{2}{\sqrt{3}} \approx 1.155$$

Equation (12) clearly indicates that in the proposed SVM scheme, sum of modulation indices increases about 15% a very important feature to provide higher torque for a given input dc-voltage. In the case of washing machines, the above capability translates to higher machine capacity (in terms of cloth load) at high spin speed (e.g., 1800 r/min) an important product feature in marketplace.

$V_{ref\,U}$ in I. III or V						$V_{ref\,L}$ in I, III or V				
V_{13}	V_{AU_2}	V_{AU_1}	V_{AU_1}	V_{AU_2}	V_{13}	V_{AL_1}	V_{AL_2}	V_{AL_2}	V_{AL_1}	V_{13}
$\frac{T_o}{2}$	T_2	T_1	T_1	T_2	T_o	T_3	T_4	T_4	T_3	$\frac{T_o}{2}$

$V_{ref\,U}$ in II, IV or VI						$V_{ref\,L}$ in I, III or V				
V_{13}	V_{AU_1}	V_{AU_2}	V_{AU_2}	V_{AU_1}	V_{13}	V_{AL_1}	V_{AL_2}	V_{AL_2}	V_{AL_1}	V_{13}
$\frac{T_o}{2}$	T_1	T_2	T_2	T_1	T_o	T_3	T_4	T_4	T_3	$\frac{T_o}{2}$

$V_{ref\,U}$ in I, III or V						$V_{ref\,L}$ in II, IV or VI				
V_{13}	V_{AU_2}	V_{AU_1}	V_{AU_1}	V_{AU_2}	V_{13}	V_{AL_2}	V_{AL_1}	V_{AL_1}	V_{AL_2}	V_{13}
$\frac{T_o}{2}$	T_2	T_1	T_1	T_2	T_o	T_4	T_3	T_3	T_4	$\frac{T_o}{2}$

$V_{ref\,U}$ in II, IV or VI						$V_{ref\,L}$ in II, IV or VI				
V_{13}	V_{AU_1}	V_{AU_2}	V_{AU_2}	V_{AU_1}	V_{13}	V_{AL_2}	V_{AL_1}	V_{AL_1}	V_{AL_2}	V_{13}
$\frac{T_o}{2}$	T_1	T_2	T_2	T_1	T_o	T_4	T_3	T_3	T_4	$\frac{T_o}{2}$

Figure 6. SVM with reduced number of semiconductor switching

A switchimg vector sequence for the proposed SVM is shown in Figure 6.This switching sequence is developed to reduce the the number of semiconductor switching. The zero vectors are placed just between two upper and lower active vectors. In upper active vectors, legs are in state $\{1\}$ or $\{0\}$ and in lower active vectors, legs are in state $\{1\}$ or$\{-1\}$. If $V13$ zero vector is placed between the

active vectors, minimum number of switching is required. While if *V*14 or *V*15 zero vectors are used, number of switching is increased.

There are two odd active vectors (*V*1, *V*3, *V*5, *V*8, *V*10, and *V*12) and two even active vectors (*V*2, *V*4, *V*6, *V*7, *V*9 , and *V*11) in a switching sequence. In an even active vector, two legs are in state *{1}*, while in an odd active vector only one leg is in state *{1}*. If even active vectors are placed next to *V*13, number of switching will be reduced even more (see Fig. 6).

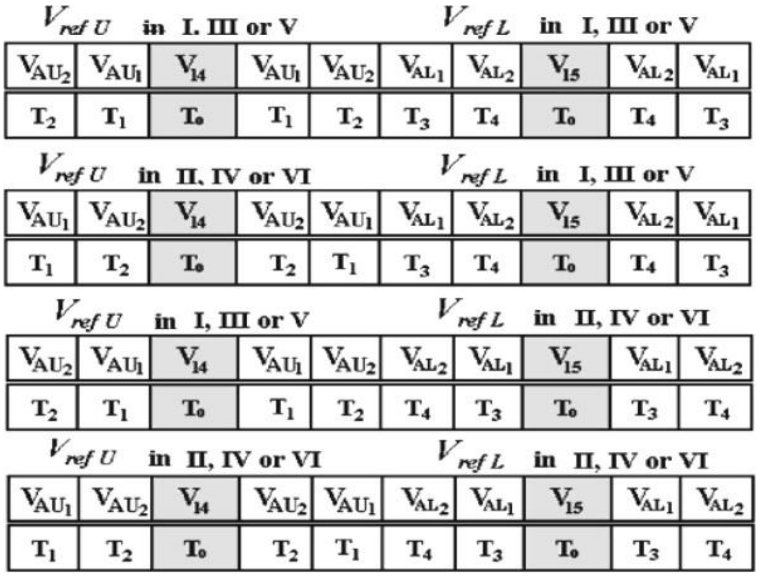

Figure 7. SVM with reduced THD

There are other possible switch generation methods too, e.g., a switching method, to reduce THD. To minimize THD, active vectors for each output should be centrally placed within the switching period. Fig. 7 shows a switching vector sequence that shifts active vector into center of switching period, hence reducing THD. In this sequence, zero vectors are inserted between active vectors. In Fig. 7, *V*14 is inserted between upper active vectors and *V*15 is inserted between lower active vectors.

IV. SIMULATIONS AND EXPERIMENTAL RESULTS

Parameter		value
Switching frequency		3kH
f_U		25Hz
f_L		50Hz
R_{load}		5ohm
L_f		5mH
Nine switch inverter	U	0.40
	L	0.50

Table 3. Simulation parameters

The proposed SVM are simulated for nine-switch inverter. Two Similar RL loads are connected to the outputs of inverter. Simulation parameters are listed in Table III. Number of switching of semiconductors for nine-switch inverter inverter using carrier-based PWM and the proposed SVMs are shown in Table IV. Number of switching for 0.1 s with parameters of Table III is calculated.

	SPWM	SVM(Minimum	SVM(Minimum
Nine-switch	3500	2400	3348

Table 4. Number of semiconductor switching

The nine-switch inverter with input dc source of 415 V is simulated and implemented with reduced number of switching SVM. Figures. 8 and 9 show line– line voltage and phase voltage of both outputs, respectively

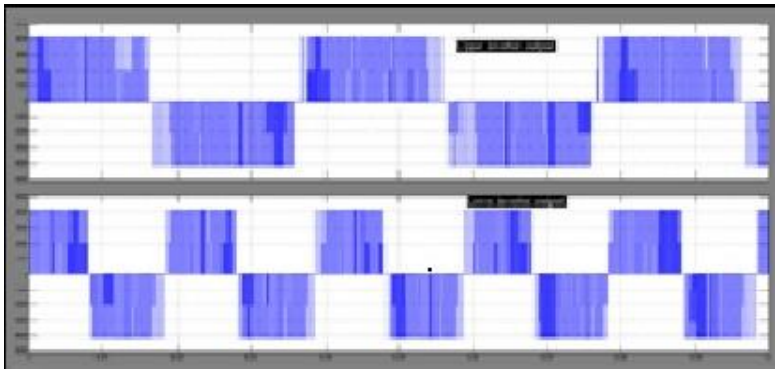

Figure 8. Line voltage of Nine-switch inverter

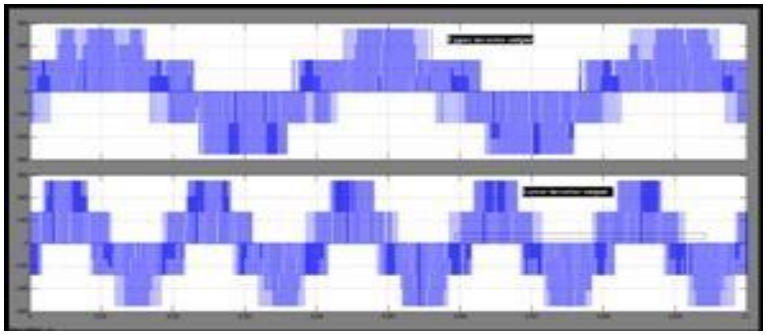

Figure 9. Phase voltage of Nine-switch inverter (min switching SVM), (100 V/DIV, 10ms/DIV).

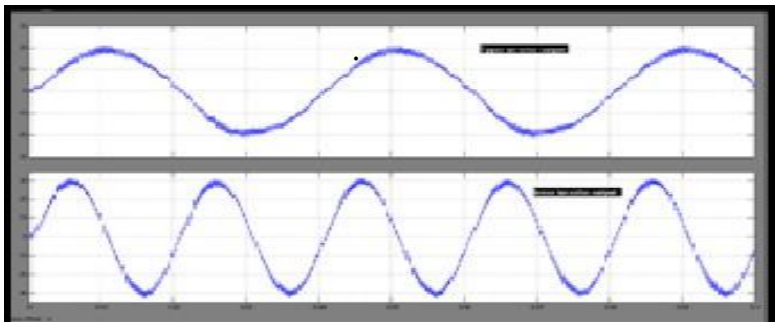

Figure 10. Output currents of Nine-switch inverter (min switching SVM). (10A/DIV, 10 ms/DIV).

It can be seen that both outputs have expected frequencies. The load current is shown in Figure 10. It can be seen that the load currents have nearly sinusoidal waveforms. Figure. 11 shows THD of load current versus load current magnitude for different cases: (a) carrier-based PWM, (b) reduced THD SVM and (c) minimum semiconductor switching SVM.

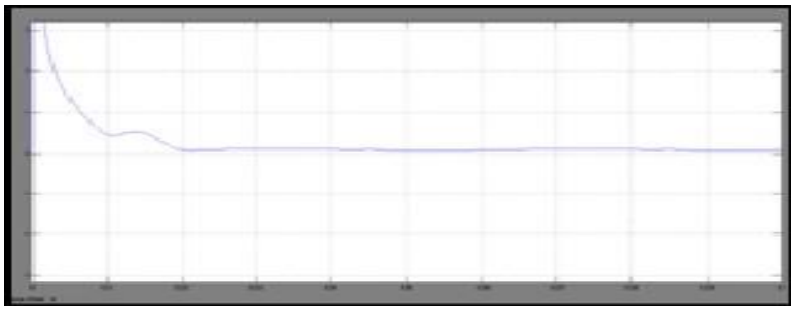

Figure 11(a). Carrier –based PWM method

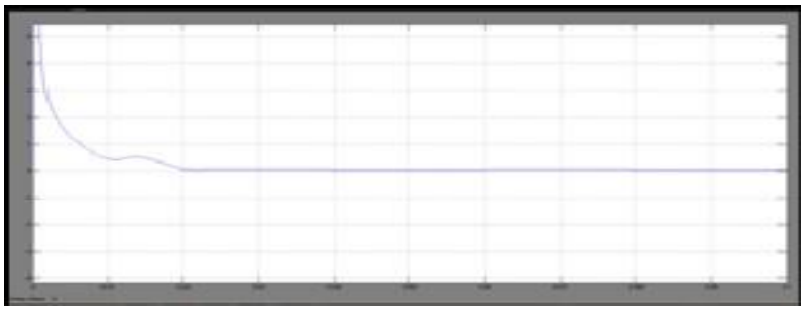

Figure 11(b). Reduced THD SVM method

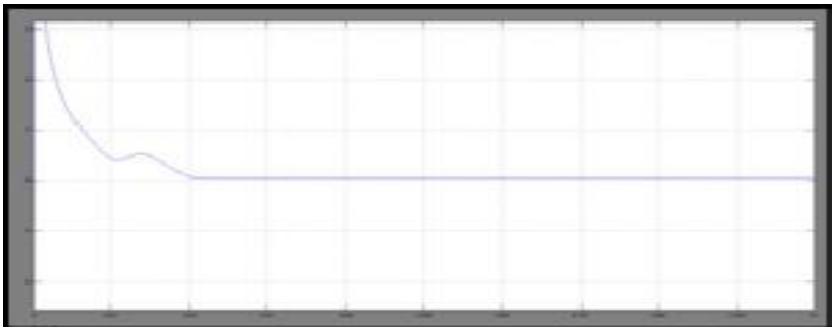

Figure 11(c). Minimum semiconductor switching SVM method

From the above simulation results THD for carrier – based PWM method is 21.27% ,for minimum semiconductor switching SVM method is 20.89% and for reduced THD SVM method THD in load current is 18.9%.

V.CONCLUSION

In this paper, the SVM of nine-switch inverter was proposed , Switching sequence of the proposed SVM is composed of the upper active vectors, the lower active vectors and the zero vectors. The upper and lower active vectors are determined via two space vector diagram. The proposed SVM increases sum of modulation indices up to 15%, an important feature in providing higher torque for a given input dc-voltage. The proposed SVMs were simulated for the nine-switch inverter, two SVM

algorithms are developed to reduce THD and number of semiconductor switching. The performance of the proposed SVMs was verified using computer simulation.

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