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Design of Reversible Synchronous Sequential Circuits

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Abstract—In early 70`s one computer requires one whole room and now a days we kept commuter in our pockets, how this happens? This happens because we did tremendous revaluation in VLSI field. We rapidly decrease size of transistors. After decades of continuous improvements and shrinking feature sizes, the development of conventional computing technologies faces enormous challenges. In particular, power dissipation in today's computer chips becomes crucial. Reversible computation is a promising alternative to these technologies, where power dissipation can be reduced or even eliminated. Reversible logic has become very promising for low power design using emerging computing technologies. A number of good works have been reported on reversible combinational circuit design. However, only a few works reported on the design of reversible latches and flip-flops on the top of reversible combinational gates and suggested that sequential circuits be built by replacing the latches and flip-flops and associated combinational gates of the traditional irreversible designs by their reversible counter parts. This replacement technique is not very promising, because it leads to high quantum cost and garbage outputs.

In this paper we design reversible synchronous sequential circuit such as counter. This design technique is directly from reversible gates using Pseudo Reed-Muller Expressions. This technique shows very much improved results In terms of quantum cost and garbage outputs.

Keywords—Reversible logic, Quantum cost, Garbage output, Ancilla inputs, Gate Level

I. INTRODUCTION

Power dissipation is one of the crucial issues in today's technology. The cause of power dissipation is loss of information and this firstly predicted by R. Landaure in 1960. According to his principal k*T*ln2 joules energy dissipate into environment when we loss one bit of information, where k is the Boltzmann's constant and k=1.38x10 -23 J/K, T is the absolute temperature in Kelvin.[1] Moore`s law said that after 18 month's transistor density on chip get doubles , if we continued with this till 2020 then it is impossible to remove heat dissipation [2] . One more researcher Bennett in 1973 showed that using thermodynamics principal, if we use loss less technology then we can reduces or eliminates power dissipation [3]. This information loss less technology is only built by reversible circuit. De Benedici [4] shows that, for power consumption reasons, reversible circuits will be the only technology possible to build supercomputers of the future. Therefore, reversibility will become an essential property in future logic circuit design and synthesis algorithms. Reversible circuits have been implemented in ultra-low-power CMOS technology[5], optical technology[6], quantum technology, nanotechnology[7], quantum dot[8], and DNA technology[9].

Most of the researcher`s work in reversible logic is only in combinational logic synthesis. Only limited attempts have been made in the field of reversible sequential circuits. Some researchers argue that we cannot implement sequential circuits in reversible logic because there is no provision for feedback loop. However, in 1980, Toffoli [10] argued that if the feedback is provided through a delay element, then the feedback information will be available as the input to the reversible combinational circuit in the next clock cycle and sequential logic is possible. There are mainly two ways for implementations of reversible sequential circuits using replacement technique [11]–[14]

and direct design using reversible gates. In this paper we design 3 bit counter using direct design technique using reversible gates. *All the results are shown in xillinx 14.5 and microwind 3.5* .

II. BACKGROUND ON REVERSIBLE LOGIC

A. Reversible Function:

The multiple output Boolean function $F(x1; x2; :::; xn)$ of n Boolean variables is called reversible if:

a. The number of outputs is equal to the number of inputs;
b. Any output pattern has a unique pre-image.

B. Reversible logic gate:

Reversible Gates are circuits in which number of outputs is equal to the number of inputs and there is a one to one correspondence between the vector of inputs and outputs[8-10]. It not only helps us to determine the outputs from the inputs but also helps us to uniquely recover the inputs from the outputs.

C. Ancilla inputs/ constant inputs :

This refers to the number of inputs that are to be maintain constant at either 0 or 1 in order to synthesize the given logical function[15].

D. Garbage outputs:

Additional inputs or outputs can be added so as to make the number of inputs and outputs equal whenever necessary. This also refers to the number of outputs which are not used in the synthesis of a given function. In certain cases these become mandatory to achieve reversibility. Garbage is the number of outputs added to make an n-input k-output function ((n; k) function) reversible.

We use the words ―constant inputs‖ to denote the present value inputs that were added to an (n; k) function to make it reversible. The following simple formula shows the relation between the number of garbage outputs and constant inputs .

Input + constant input = output + garbage. [16]

E. Quantum cost:

Quantum cost refers to the cost of the circuit in terms of the cost of a primitive gate. It is calculated knowing the number of primitive reversible logic gates (1x1 or 2x2) required to realize the circuit. The quantum cost of a circuit is the minimum number of 2x2 unitary gates to represent the circuit keeping the output unchanged. The quantum cost of a 1x1 gate is 0 and that of any 2x2 gate is the same, which is 1 [12].

F. Flexibility :

Flexibility refers to the universality of a reversible logic gate in realizing more functions [13].

G. Gate Level **:**

This refers to the number of levels in the circuit which are required to realize the given logic functions.

H. Hardware Complexity :

This refers to the total number of logic operation in a circuit. Means the total number of AND, OR and EXOR operation in a circuit [14]

I. Reversible Logic Gates

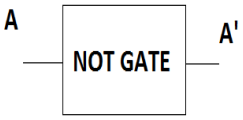
There are many number of reversible logic gates that exist at present. The quantum cost of each reversible logic gate is an important optimization parameter [16]. The quantum cost of a 1x1 reversible gate is assumed to be zero while the quantum cost of a 2x2 reversible logic gate is taken as unity. The quantum cost of other reversible gates is calculated by counting the number of V, V+ and CNOT gates present in their circuit. V is the square root of NOT gate and V+ is its Hermitian. The V and V+ quantum gates have the following properties:

V * V = NOT ..... (1)
V * V+ = V+ * V = 1 ..... (2)
V+ * V+ = NOT ..... (3)

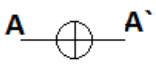
Some of the important reversible logic gates are,

1) NOT Gate :

The simplest Reversible gate is NOT gate and is a 1 x 1 gate[7]. The Reversible 1x1 gate is NOT Gate with zero Quantum Cost is as shown in the Figure 1.



(a) Block diagram

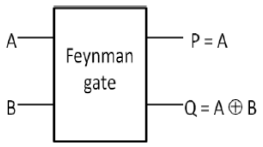


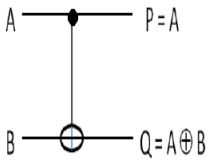
(b) Logic circuit

Figure 1. NOT gate

2) FEYNMAN Gate (CNOT GATE)

FEYNMAN Gate is also known as Controlled-Not Gate. It is a 2x2 reversible gate. The CNOT gate can be described as: Iv = (A, B) ; Ov = (P= A, Q= A B) Iv and Ov are input and output vectors respectively. To design a cnot gate we require only one primitive gate so Quantum cost of CNOT gate is 1[17]. Figure 2 shows a 2x2 CNOT gate and its symbol.





A	B	P	Q
0	0	0	0
0	1	0	1
1	0	1	1
1	1	1	0

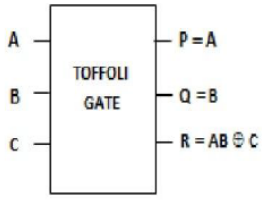
(a) Block diagram *(b) Logic circuit* *(C) Truth Table*

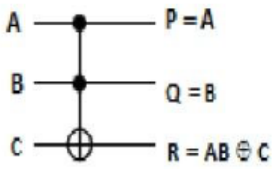
Figure 2: CNOT Gate

3) TOFFOLI Gate: (CCNOT Gate)

TOFFOLI gate which is a 3*3 gate with inputs (A, B, C) and outputs P=A,Q=B, R=AB XOR C.

It is also called as Control control not gate (CCNOT). It has Quantum cost five[21].





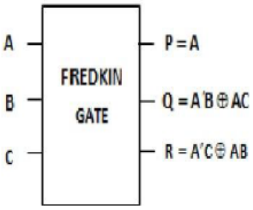
A	B	C	P	Q	R
0	0	0	0	0	0
0	0	1	0	0	1
0	1	0	0	1	0
0	1	1	0	1	1
1	0	0	1	0	0
1	0	1	1	0	1
1	1	0	1	1	1
1	1	1	1	1	0

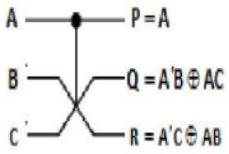
(a) Block diagram *(b) Logic circuit* *(C) Truth Table*

Figure 3: Toffoli Gate

4) FREDKIN Gate:

Fredkin gate which is a 3*3 gate with inputs (A, B, C) and outputs P=A, Q=A'B+AC, R=AB+A'C. It has Quantum cost five[22].





A	B	C	P	Q	R
0	0	0	0	0	0
0	0	1	0	0	1
0	1	0	0	1	0
0	1	1	0	1	1
1	0	0	1	0	0
1	0	1	1	1	0
1	1	0	1	0	1
1	1	1	1	1	1

(a) Block diagram *(b) Logic circuit* *(C) Truth Table*

Figure 4: Fredkin Gate

III. DESIGN OF COUNTERS

In this section we discuss designs of practically important synchronous counters using the direct design technique. From [15] and [16] we gate following equation for 3 bit counter

$$Q2+ = Q2 \oplus CQ1Q0 \quad \ldots\ldots\ldots\ldots (1)$$
$$Q1+ = Q1 \oplus CQ0 \quad \ldots\ldots\ldots\ldots (2)$$
$$Q0+ = Q0 \oplus C \quad \ldots\ldots\ldots\ldots (3)$$

The circuit diagram for above equation is shown in Figure 5. The circuit requires one 4×4 Toffoli gate, one 3×3 Toffoli gate, and four Feynman gates. Thus, the realization cost of mod 8 up counter is 19. The only unused output is the *C* output. In addition, the 4×4 Toffoli gate requires one garbage output. Thus, the total number of garbage outputs of this design is two.

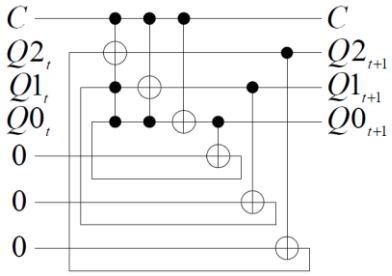


Figure 5: 3 bit counter using Reversible Gates

IV. RESULTS

In this section we discuss the results of 3 bit counter. All the results are in xillinx 14.5 and microwind 3.5.fig 1 shows the output in xillinx and fig 2 output in microwind

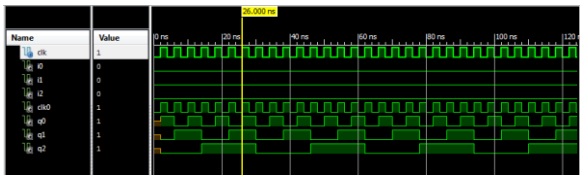


Figure 6: Output 3 bit counter in Xillinx 14.5

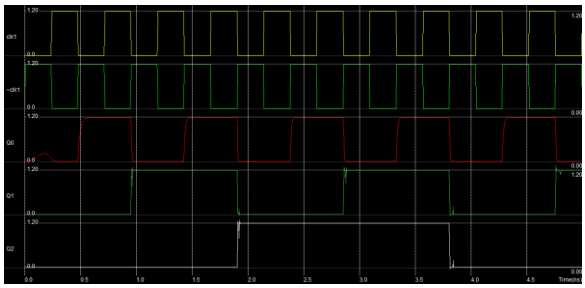


Figure 7: Output 3 bit counter Microwind

V. CONCLUSION

Reversible logic has shown a good promise for low-power design using emerging computing technologies. A good number of design methods for reversible combinational circuits have been proposed . However, only a very limited works have been reported on reversible sequential circuit design. In this paper, we present a novel approach of direct design of sequential circuit with reversible gates using PSDRM expressions describing the state transitions and output functions of the circuit. Design examples show that our direct designs save 1.54%–49.09% quantum cost and 51.43%–81.82% garbage outputs than the replacement design approach suggested earlier. Thus, our proposed direct design method outperforms the previously reported replacement design approach.

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