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ANALYSIS AND DESIGN OF LOW VOLTAGE LDO WITH CMOS SUPER SOURCE FOLLOWER

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Abstract-In this paper a low voltage, low drop-out (LDO) voltage regulator design is implemented using 250 nm Technology. Here the design of the Low Voltage LDO comprises of two stage Error Amplifier (EA), CMOS Source follower, Power Mosfet (Mp) and Feedback Network. The main purpose of the design is to operate in low Voltage i.e 1V. The drop voltage of this design is less than 100mv that is 0.081mv. The experimental result shows that the Quiescent current (Iq) is 0.8µA, Power dissipation is 80pW and the regulated output voltage is 0.919mV. This design is build using 22 number of transistors only. This is the best achievement of the design.
Index Terms: low drop-out, low-voltage regulators, CMOS, power mosfet, CMOS super source follower, two stage error amplifier.

I. INTRODUCTION

Each electronic component having the power supply section that consist of some blocks. Various multimedia and portable device needs low power consumption, high performance and compactness all at same time. The important issue to design of power management module that is low power consumption for extending battery life time.

Regulator will plays the important role to produce the stable/constant output voltage. It has switching regulator and linear regulator. A linear regulator is easy to integrate on-chip within a small area [3]. LDO the name itself it identify the dropout voltage should be low. So we can easily increase the battery life. By this we will achieve the VLSI primary goal. The

difference between the unregulated input voltage and regulated output voltage is known as drop voltage.

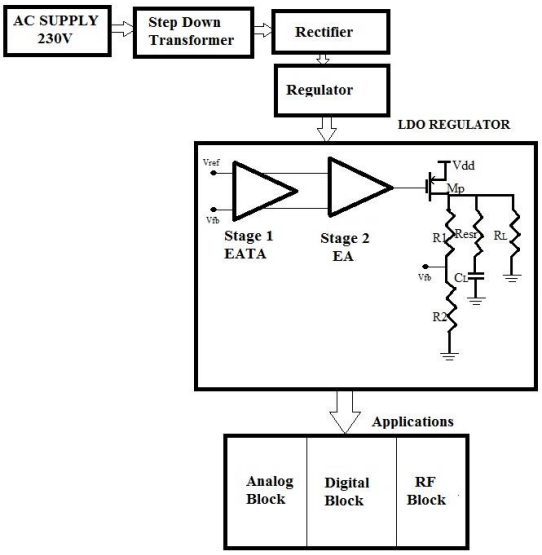

Fig. 1. Power Supply Section Using Proposed LDO.

II. EXISTING SYSTEM

In the existing system design is comprised of two stage error amplifier (EA), Transient Accelerator (TA), Power Mosfet (Mp) and feedback network. Schematic diagram is shown in fig 2. But the primary focus of this project is to operate in low voltage i.e. 1V. Output of this designed regulator is 0.85V. so the voltage drop of this design is 150mV.

A. Error Amplifier

A simple symmetrical Operational Transconductance Amplifier (OTA) is used as the Error Amplifier. The OTA is an error amplifier whose input voltage produce an output current so it's called as Voltage Controlled Current Sources (VCCS).

$$I_{OUT} = (V_{in+} - V_{in-}).g_m \quad (1)$$

The amplifier's output voltage is the product of its output. Current and its load resistance shown in equ (2).

$$V_{out} = I_{out} \cdot R_{load} \quad (2)$$

The transconductance of the amplifier is usually controlled by an input current denoted by I_{abc} is composed of M_{EA1} – M_{EA9}. The OTA type EA requires no compensation capacitor and operate in minimum supply voltage (Vdd, min) equal to one threshold voltage pluse twice the overdrive voltage (V_{ov}) = V_T+2*V_{OV} . It achieves rail to rail output swing by the output stage M_{EA7}, M_{EA9}. Size of Mp is reduced for specific load current requirement. so, significantly it reduce the circuit area and smaller gate capacitance.

B. Transient Accelerator

Increasing the charging and discharging current during the load transient we can reduce the slew time of the gate Mp. the EA is reused consider as stage 2 it will detect the output variation of the TA. When the

output voltage (Vout) and feedback voltage (Vfb) is variations occur, the load changes largely. Feedback Voltage (FB) is amplified by the output variation detector of the transient accelerator.

C. Power MOSFET

- Achieve high speed switching operation.
- It generate low noise.
- Capable for operate up to 100MA.
- Designed for high volt operation.

The low on-resistance and high current carrying capability of power MOSFET make them preferred switching devices. Unlike bipolar transistors, power MOSFETs have a considerable gate capacitance that must be charged beyond the threshold voltage (device is ON), V_{GS} (Mp), to achieve turn-on.

The total gate charge, Q_G, that must be dispensed into the equivalent gate capacitance of the MOSFET equation (3) to achieve turn-on Mp is given as:

$$Q_G = Q_{GS} + Q_{GD} + Q_{OD} \quad (3)$$

Where
Q_G is the total gate charge
Q_{GS} is the gate-to-source charge
Q_{GD} is the gate-to-drain Miller charge
Q_{OD} is the "overdrive charge" after charging the Miller capacitance.

Generally PMOS is the biggest component, usually the aspect ratio W/L is greater than some tens of thousands and generally the minimum length channel is used to achieve the drop-out specification that requires a large aspect ratio. For low voltage operation a P-type is chosen to construct the power mos transistor Mp.

III. CIRCUIT REALIZATION

Stage1 is the combination of EA and TA, is Cascaded with stage 2 Error Amplifier. The Error Amplifier also the output will depends on Ref. voltage (Vref) and Feedback voltage (Vfb)

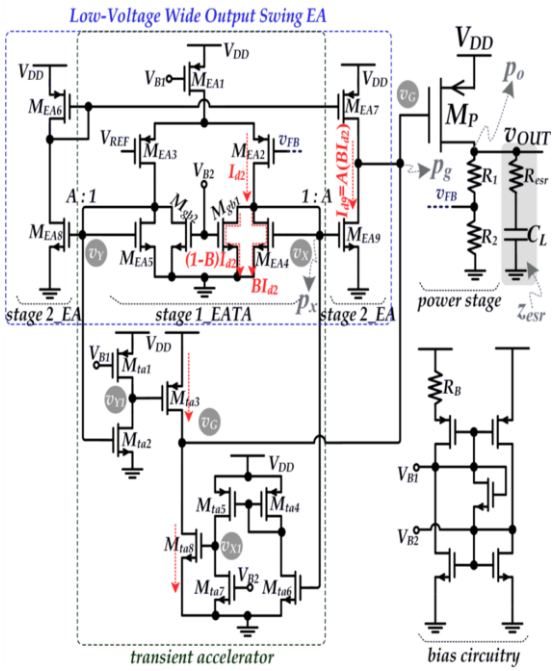

Fig. 2. Circuit Diagram of the Existing System

Our goal of this circuit is to operate in low voltage also to produce the fast transient response. By using the EA, it achieve low voltage to achieve accurate output. To reduce the area, we use the EA, to replicate the power noise instead of using an auxiliary circuit. The two equivalent resistors between the output node Vx and Vy of the first stage of the EATA. The ground have a low resistance value 1/gm4 and 1/gm5. So the power noise of stage 1 EATA (Error Amplifier and Transient Accelerator) can be attenuated at node Vx and Vy. Only a small level of power noise can be coupled Vx and Vy as they appear in the form of common mode input to the output stage of EA. This Common Mode (CM) noise signal Vicm and cause a fluctuation on Vg6. The output Vg is induced by Vicm. Stage1 gain is too low to achieve a fast transient response. To increase the gain use stage 2 is to overcome this by current splitting technique will apply.

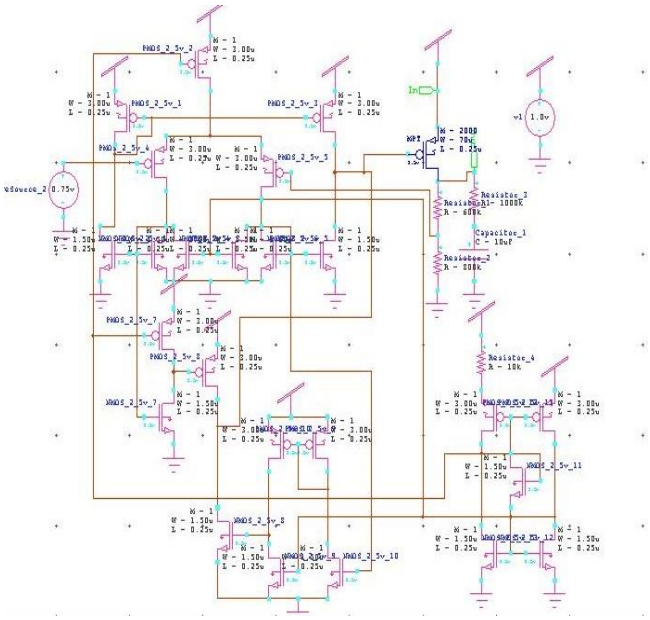

Fig.3. Schematic Diagram of the Existing System.

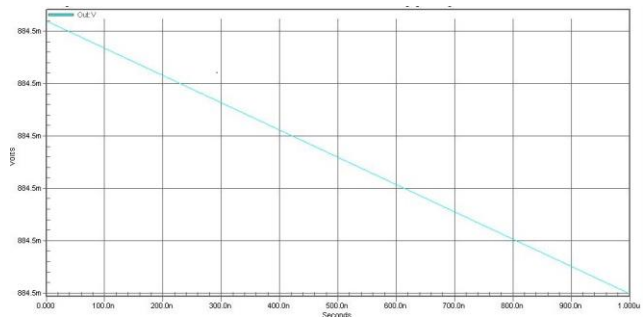

Fig.4. Transient Response.

The schematic diagram is shown in figure 4 and related transient response is shown in figure 5.

IV. PROPOSED SYSTEM

In the proposed system comprises of two stage error amplifier (EA), CMOS Super Source follower, Power Mosfet (Mp) and feedback network. Schematic diagram is shown in fig 5. But the primary focus of this project is to operate in low voltage i.e. 1Voltage Output of the regulator is 0.919V So the voltage drop of this design is 0.081V.

i) CMOS Super Source Follower

Due to the large parasitic capacitance at the gate of the pass element, a voltage buffer is usually inserted between the error amplifier and the power MOSFET.

The buffer isolates the capacitance from the high impedance at the error amplifier output, which will extends the bandwidth of the LDO. It also increases the slew rate of the error amplifier, further

improving the LDO's transient response.The PMOS source follower buffer in Fig. 3 (b) eliminates I_b and and reduces r_o through feedback. The output impedance of the buffer is approximately [2]

$$r_o = \frac{1}{g_{m1}(1+\beta)} \qquad (4)$$

As such, both buffers require bipolar transistors. Though BiCMOS technologies provide high performance bipolar and CMOS transistors, the construction of NPN BJTs in a CMOS technology usually require a twin-well process. Furthermore, the vertical parasitic NPN may not have a high enough forward current gain β to reduce the output impedance effectively, as seen in Eq. 4. Its output impedance can be derived through inspection. If the body effects can be ignored and $r_o1, r_o2 \rightarrow \infty$, a voltage step Δv applied at the output will change the voltage at node X to

$$v_x = g_{m1} r_{o1} \Delta v \qquad (6)$$

$$\Delta i = g_{m2} v_x \qquad (7)$$

$$\therefore r_o = \frac{\Delta v}{\Delta i} = \frac{1}{g_{m1}} \frac{1}{g_{m2} r_{o1}}$$

Eq. 5 is in agreement with a detailed analysis based on the small-signal equivalent circuit [5]. Finally, the choice of I2 given the the total quiescent current budget I1 is not trivial. It can be shown that I2 = 1/2I1 achieves the minimal ro.

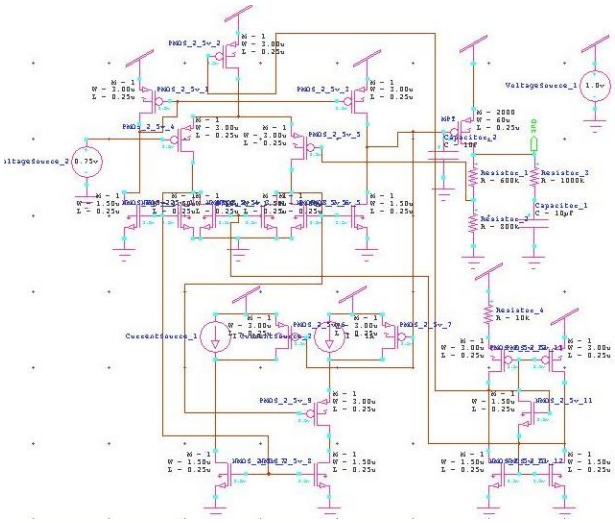

Fig.5. Proposed Schematic Diagram

The full schematic of the proposed LDO is shown in Fig. 5.6. Here the two stage error amplifier collects the Reference Voltage and Feedback Voltage. Stage1 EA is used to operate the circuit with low voltage and stage 2 EA is avoid the noises and attention. The output of the error Amplifier has good output swing to drive Power Mosfet. But the Resistance value is high. To decrease this resistance value use Super Source Follower. Normally Power Mosfet has capability to operate high load current. To satisfy this we need to produce the low output resistance to the gate of the power mosfet.

V. SIMULATION RESULT

The proposed LDO was designed and implemented in a Generic 250 nmCMOS process. The LDO is designed to operate under 1 V input and regulates 0.919 V output.

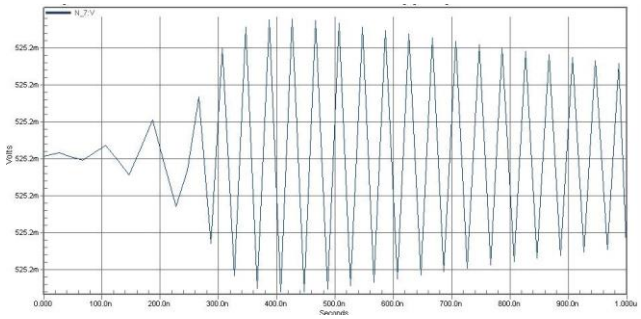

Fig.6. Feedback Voltage Waveform.

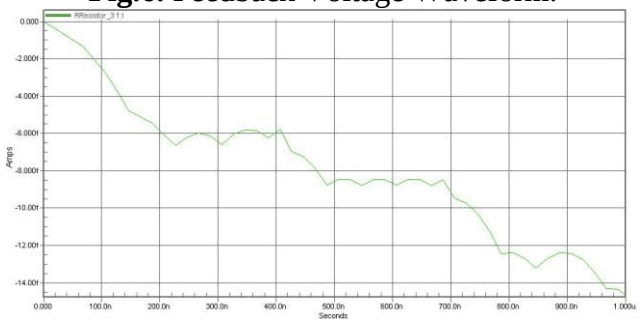

Fig.7. output current with load

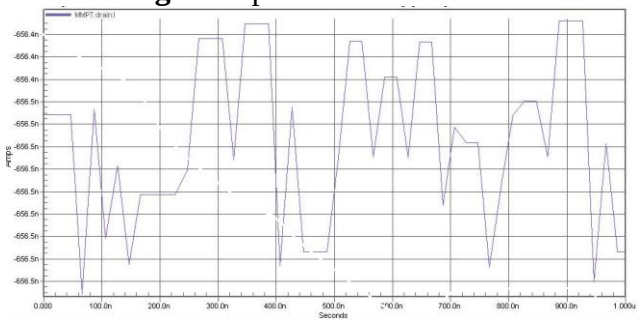

Fig.8. output current without load

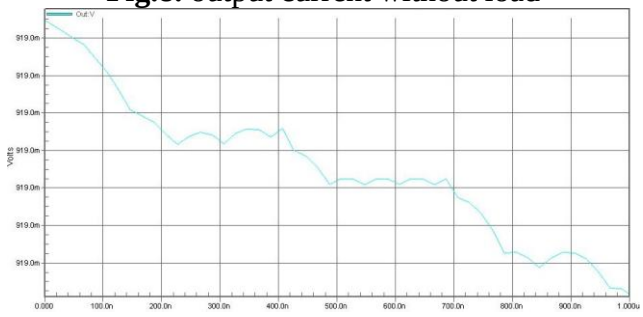

Fig.9. Transient Response of the proposed design

VI. COMPARISION

The comparison between the existing and proposed design is sown in Table 1. And also the Fig. 10 shows the graph view for the difference between the Input Voltage, Drop Voltage and Output voltage. In Fig.11 shows the difference between the number of transistor in existing and proposed system.

PARAMETERS	EXISTING SYSTEM	PROPOSED SYSTEM
Technology	Generic 250nm	Generic 250nm
Vdd	1V	1V
Vout	0.884V	0.919V
Drop voltage	0.186V	0.081V
Input Current	84.58µA	83.63µA
Feedback Voltage	499.7mV	525.2mV
Reference Voltage	0.75mV	0.75mV
Iq With Load	1.19A	0.8µA
Iq Without Load	0.839µA	0.849µA
Power Dissipation	0.1512W	8pW
No. of Transistors	25	22

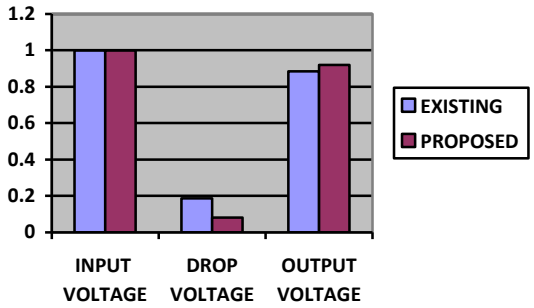

Fig.10. Comparison between input, drop and output

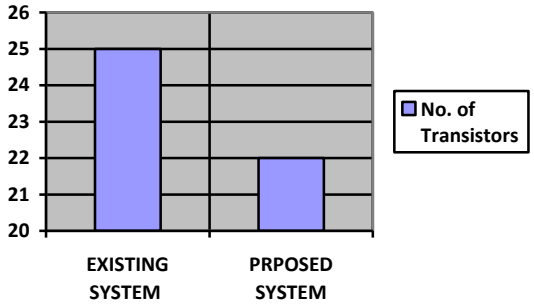

Fig.11. Comparison of number of transistors used.

VII. CONCLUSION

This project successfully simulated and analyzed the transient response and also to calculate the total power dissipation, Quiescent Current. The main achievement of the design is to operate in low 1 Volt and drop voltage of the design is 0.081V, due to the minimum drop voltage we can easily increase the battery life without affecting the stability. Finally, the measured response of the total Power Dissipation is 8pW, and the Quiescent Current (Iq) is 0.8µA.

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