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Design of Asynchronous Viterbi Decoder using Bundled Data Protocol for Low Power Consumption

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Abstract - The main aim of this article is to design Asynchronous Viterbi Decoder for getting low power consumption and increasing the speed. Fast developments in the stream of communication have increasing demands of low power and high speed decoders with low circuit implementation. In this paper, Asynchronous Viterbi Decoder has been implemented with code rate of r=1/3 and constraint length K=3 and the simulation results are operated by using VHDL in Model Sim SE 6.1f tool. This paper also focuses on the study of different sections of Viterbi Decoder. For the Asynchronous design, Bundled data protocol is used in this paper. Asynchronous designs have many benefits over the Synchronous designs.

Keywords: Viterbi Decoder, Convolutional Encoder, Asynchronous Viterbi Decoder, Synchronous Asynchronous Systems, Bundled Data Protocol

I. INTRODUCTION

Viterbi Decoding algorithm is an extract recursive algorithm for creating the shortest path through a trellis. Viterbi Decoder is used to encode the information through convolutional encoder and transmitted over the noisy channel. Viterbi Decoder have wide applications in Wireless Communications, Digital Television Broadcasts, pattern as well as speech recognition and large applications in cell phones etc.

Viterbi decoders can be implemented with two designs first is with synchronous design and another is with Asynchronous design. Synchronous designs means in that system they share common and discrete notion of time which is defined by clock signal throughout the system. And due to this, majority of the systems are based on synchronous principle. The process of enforcing an ordering of events on signals is called as synchronization. Since, in the synchronous designs longest path in the combinational logic determines the minimum clock period; these systems have to face problems with global clock distribution. However it leads to skew problems. Also during every clock cycle, each register dissipates large power. These types of problems are created in synchronous designs.

On the other hand, Asynchronous designs are build up with blocks that communicate to each other using handshaking signals. The process of performing the synchronization, communication, and sequencing of operations is called as Handshaking. In the Asynchronous designs, circuit components do not share the common and discrete time. Asynchronous designs are locally, rather than globally synchronized and for performing the necessary synchronization they uses handshaking signals. Asynchronous designs have many advantages over the Synchronous designs. Due to fine-grain clock gating and zero standby power consumption they consume low power. Since the operating speed is determined by local latencies, they can maintain high speed. Due to the simple handshake interfaces and the local timing Asynchronous system possess better compensability and modularity. In the consequence of there is no global signal, these systems do not face the problems of clock distribution and clock skew. Because of the local clocks tries to tick at random points in

time, less electromagnetic emission noise achieved in these circuits. Due to these advantages design of Asynchronous system has thus become attractive for digital system designers during past few years.

II.CONVOLUTIONAL ENCODER

There has been fast increment in the implementation of high speed Viterbi Decoders for convolution codes, in recent years. Convolution codes have excellent error –control performance. Therefore in most of the communication systems they are widely used. In this paper encoder of code rate r=1/3 and constraint length K=3 with input bit k=1 is implemented. The block diagram of Convolution Encoder is as below in figure 1. This Encoder consists of three shift registers and two Xor gates. And for one input it gives three output equations i.e. out 0,out 1 and out 2.

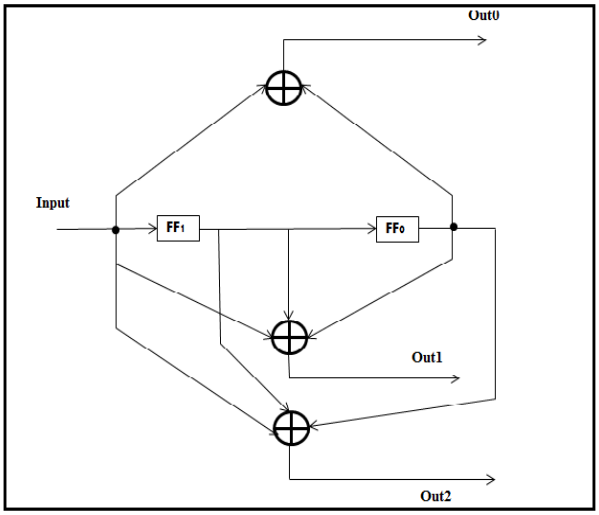

Figure1. Convolutional Encoder (K=3, k=1 and n=3)

Out o = Input Xor FF0
Out1 = Input Xor FF1 Xor FF0
Out2 = Input Xor FF1 Xor FF0
In this paper, for the input sequence'011010111100', output sequence 000,111,100,100,000,011,000,100,011,100,111 is obtained.

III. VITERBI DECODER

Viterbi Decoder is composed of following three major sections which are shown in the figure 2. i.e.

- Branch Metric Unit (BMU),
- Add Compare Select Unit(ACSU) and
- Survival Path Memory Unit(SMU).

BMU block is composed of Xor gate and counter. Branch Metric Unit calculates branch metrics by using hamming distances and send to the ACSU unit. Add Compare Select Unit calculates the summation of branch metric from BMU and previous state metric which are called as path metric and send to the next block SMU. Survival path memory unit updated value of each state and then shortest path is selected by comparing previous state metric.

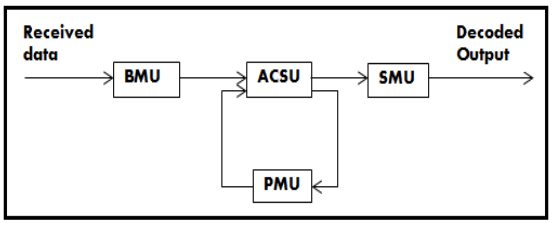

Figure 2. Viterbi Decoder

IV.PROPOSED ASYNCHRONOUS VITERBI DECODER

Asynchronous designs are more beneficial than Synchronous design therefore in recent years systems are designs with Asynchronous design. In order to reduce the power consumption and increase the speed Asynchronous Viterbi Decoder have to designed. And in this paper Asynchronous technique is implemented by using Bundled data protocol. There are two types of encoding schemes- Bundled data protocol and Duail rail protocol. In this paper, Bundled Data Protocol is used to design the system Asynchronous. Figure 3 shows bundled data protocol. For encoding the information, bundled data protocol use normal Boolean levels and they also uses separate request and acknowledge wires bundled with data signals. The function of the request wire is to inform the validity of data on the data bundle to the receiver. There are two types of Bundled Data Protocol- a) 4-Phase Bundled Data Protocol and b) 2-Phase Bundled Data Protocol.

In Bundled data protocol, data is transmitted through one wire per bit information hence it is called as Single-Rail encoding. The 4-phase bundled data protocol depends on level signalling. And it refers to four communication cycles. While 2-phase bundled data protocol depends on transition signalling.

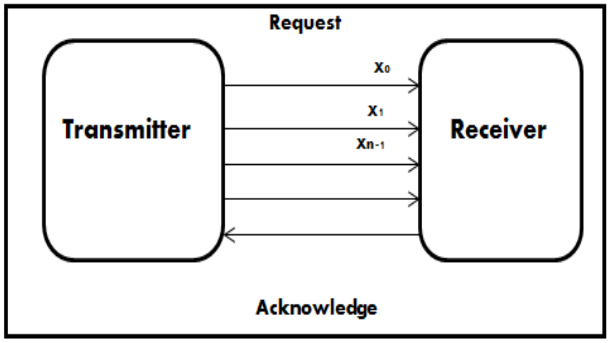

Figure 3. Bundled Data Protocol

As compared to 4-phase, 2-phase bundled data protocol is faster than 4-phase bundled data protocol; but it has more complex circuit implementation. Therefore, 4-phase bundled data protocol is used in this paper. And results are simulated in Model Sim SE 6.1f tool by using VHDL. Architecture of proposed Viterbi system is shown in figure 4.

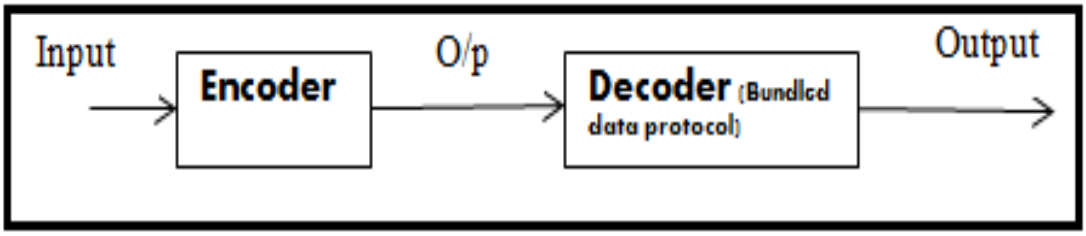

Figure 4. Proposed Asynchronous Viterbi Decoder

V. SIMULATION RESULT

This is a simulation result of bundled data protocol for input sequence 011010111100 in Model Sim 6.1f tool.

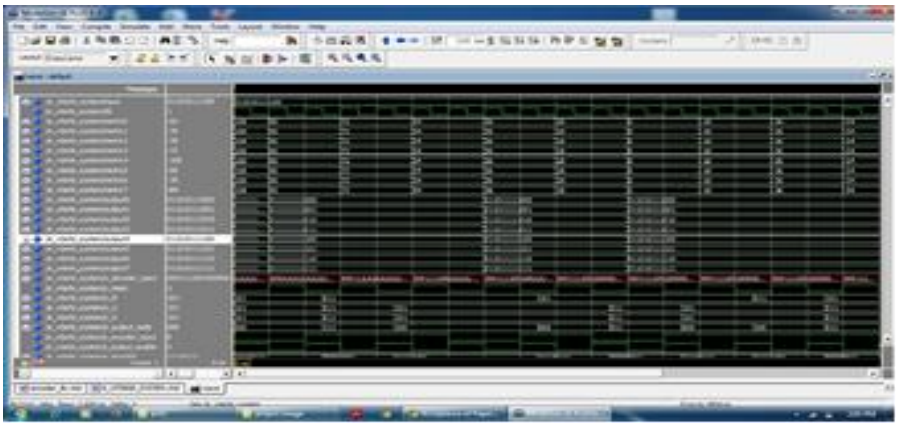

Figure 5. Simulation Result of Asynchronous Viterbi Decoder using 4-phase Bundled Data Protocol

VI. CONCLUSION

Viterbi Decoder applied in digital communication are complex in its implementation and dissipate large power. To reduce the power consumption and maintain the speed Asynchronous Viterbi Decoder is required. In this paper, Asynchronous Viterbi Decoder of code rate r=1/3 and constraint length K=3 is implemented by using 4-phase Bundled Data Protocol. The complete design was carried out using VHDL and implemented in Model Sim SE6.1f tool. And also all the components of Viterbi Decoder is properly studied.

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