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Asymmetrical Dual Bridge 7-level Dc-Link Inverter Topology

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Abstract— Multi-level inverter has a capability to reduced voltage stress across power switches and low total harmonic distortion (THD) output voltage waveform. The variable voltage and frequency requirements the need and increasing trend of using multilevel inverter (MLI) in modern drives and utility applications. The MLI curves nearly sinusoidal output voltage waveforms like that stair case voltage waveform depend of steps. The proposed topology is reduced the size, cost and complexity of the circuit. The paper orients to develop a new variety of dual bridge multilevel inverter (DBMLDCLI) with primary objective to arrive at reduced component count for particular voltage level. By appropriately choosing ratio of voltage sources (Vo:Vn) and connecting parallel to H-bridge with diode, where H- bridge used for increased no of level and diode for current path. This paper present a novel multilevel topology witch is capable of obtaining all additive and subtractive combinations of input DC voltage. The numbers of level depend on DC source arrangement. For this proposed topology different PWM techniques are used for control the switches of the inverter. The performance of the proposed topology is analyzed through MATLAB based simulation studies.
Keywords — Multi-level inverter (MLI), Multi-level DC-link inverter (MLDCLI), THD.

I. INTRODUCTION

In recent years multi-level inverter is used in large amount in industry. For high voltage and high power quality applications. The first 'Multilevel inverter' introduced in years 1970s and 1980s. The term multilevel inverter basically start from three level inverter that can used in high power medium voltage application due to its advantages over the two level inverters such as. Low switching frequency hence reduction in switching losses, lower common mode voltage.MLI inverter output voltage waveform is stair case type waveform which like that sinusoidal waveform. MLI inverter has disadvantages that by increasing the number of voltage levels, higher number of semiconductor switches required with separate gate driver circuit. Due to this it increase the size and complexity of the circuits different pulse-width modulation techniques are used to control the switch of inverter.

MLI are used in adjustable speed ac drive, induction heating, stand by aircraft power suppies, UPS (uninterruptable power supplies), HVDC transmission lines etc. MLI are preferred for high power and medium voltage application like static reactive power and medium voltage application like static reactive power compensation.MLI is reduced harmonic content in output side, lower blocking voltage in the switching devices and dismissed losses due to less commutation stress [1-8].They used for high power drives and reactive power compensation due to their ability to offer higher voltage from medium voltages dc-link and less distortion output voltage [9-17]. Multilevel DC-link inverter (MLDCLI) improved performance of two level inverter [18].MLI is reduced total harmonic distortion content in output side so technical and economical barrier like the cast of drive and protection, stable dc supply voltage and packing, the number of inverters to be limited.

Several MLI conventional topologies have been classified as diode-clamped [1,19], capacitor-clamped converter[20,21], cascade H-bridge converter [22]. These inverters are increased number of level with reduced number of switches and gate driver circuit. Conventional multilevel inverters drawbacks are inconveniences operating with balancing capacitor [5, 23]. In case of series parallel DC-link inverter reduced distortion of power switches and eliminates the necessity of capacitors [24]. In this paper develop a new class of MLDCLI topology namely dual bridge multilevel DC-link

inverter (DBMLDCLI) which required for reduced distortion of output voltage and less number of power switches. In this topology two H-bridge is used for increased the number of level and another bidirectional power flow. This paper present 7 level multi level inverter with different PWM technique which is used for control the switches of inverter. It seeks the role of phase opposition disposition (POD) multi-carrier pulse width modulation(MC-PWM) strategy implement using different output voltage level for 7-level inverter can be obtained by MATLAB/SIMULINK software[25].

II. MULTILEVEL INVERTER TOPOLOGY

1. CONVENTINAL TOPOLOGIES

1. CASCADED H-BRIDGE MULTILEVEL INVERTER:-

A cascaded multilevel inverter consist of series connected single full bridge inverter with own isolated dc sources. DC voltages source are obtained from solar cells, fuel cells batteries, ultra capacitor, etc. In this type MLI does not need any transformer nor flying capacitor. Fig-1 seven level cascade h-bridge MLI consist of three cell of h-bridge each cell has built to four switches and generate three different outputs voltage +Vdc,0 and – Vdc by connecting the ac output.

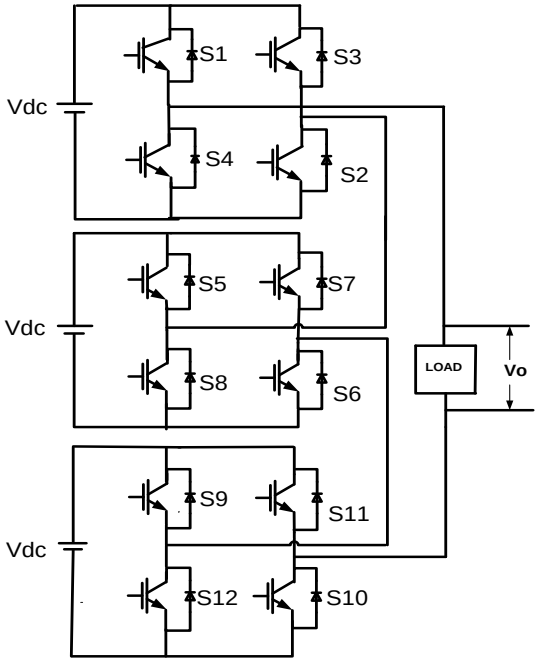


Figure 1: Seven-Level Cascaded H-Bridge MlI.

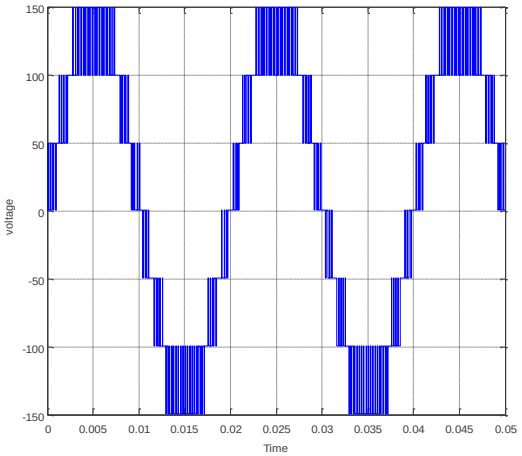


Figure 2: Output phase Voltage Bridge MlI. Waveform Of 7-Level H-

The output voltage level can be expressed using the relation M = (N+2)/2 where N is number of switch and M is number of voltage Level. The resultant output of M level inverter is sum of individual cell output. The resultant output voltage level of seven level inverter are +3Vdc to -3Vdc witch waveform is stair type as shown in figure 2. In seven level cascade h-bridge multilevel inverter has built to twelve IGBT switch and three dc voltage source each source same value of voltage Vdc = 50V .Advantages of H bridge multilevel inverter are, first stress on each switch is decreases therefore the rated voltage and the total power of the inverter are safely increases, second rate of change of voltage (dV/dt) is decreases, third cause of more output level harmonic distortion is decrease, fourth lower electro-magnetic interference (EMI) is obtain. This topology also used for three-phase MLI with the same principle. Seven-level cascaded h-bridge MLI is a symmetrical topology because all the value of separate dc source is same.

2. DIODE-CLAMPED MULTILEVEL INVERTER:-

Diode-clamped MLI is also called as neutral-point clamped inverter. Neutral-point clamped inverter was first introduced by Nabae, Takahashi, and Akagi in 1981 was essentially a three-level diode clamped inverter [6]. In this topology all the power switches are connected in series with each other. In this topology one dc sources is needed and (N-1) capacitor is used to divide the dc link into different voltages levels, where N is numbers of levels. The clamping diode is used to block the current and their number is selected in such a manner to have the same block voltages. The middle point of (N-1) capacitor is defined as the neutral point. In 7-level diode-clamped MLI as shown in Figure 3, a dc bus voltage which consists of six capacitor: C1, C2, C3, C4, C5 and C6 and each bulk capacitor has a dc voltages Vdc/6. It can be used for N levels of voltages by increasing the number of capacitor. The resultant output voltage is given by +Vdc/6, +Vdc/3, +Vdc/2, 0, -Vdc/6, -Vdc/3, and -Vdc/2 which gives staircase waveform as shown in Fig.4. For N-levels of diode-clamped MLI 2(N-1) switching devices, (N-1)*(N-2) clamping diode and (N-1) dc link capacitor are required.

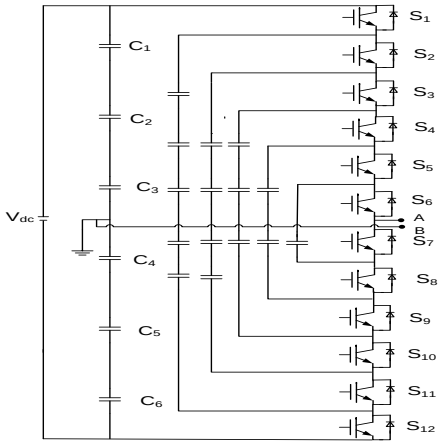


Figure.3: Single phase 7-level diode-clamped MLI.

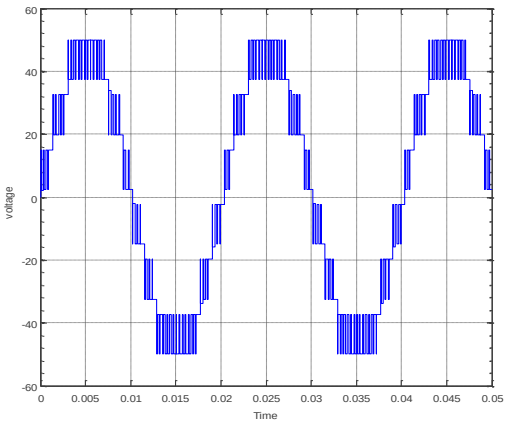


Figure 4: Output phase voltage waveform of 7-level diode-clamped MLI.

1. FLYING-CAPACIOR MULTILEVEL INVERTER:-

Flying-capacitor MLI was first introduced by Meynard and Foch in 1992[MLI chapter book]. The basic circuit diagram of flying-capacitor MLI is similar to that of diode-clamped MLI but in the place of camping diode these MLI uses extra capacitor to clamp the connecting point of semiconductor devices which are connected in series. In this topology clamped capacitor is connected in series to block the current and their number in each leg is taken in such a manner that all capacitor store same amount of energy. Flying-capacitor can be extended for generating N voltage levels by adding the capacitor. For N-levels flying-capacitor MLI 2(N-1) switching devices, (N-1)*(N-2)/2 clamping capacitor and (N-1) dc link capacitor are required. In 7-levels flying-capacitor MLI as shown in Figure 5 requires one dc source and six clamping capacitor C1 to C6 and each bulk capacitor has a dc voltage Vdc/6. The resultant output voltage is given by +Vdc/6, +Vdc/3, +Vdc/2, 0, -Vdc/6, -Vdc/3, and -Vdc/2. Which gives staircase waveform nearly to sinusoidal waveform as shown in Fig.6. These three conventional topologies has same number of count of semiconductor devices due to which more gate circuit required and circuit become complex.

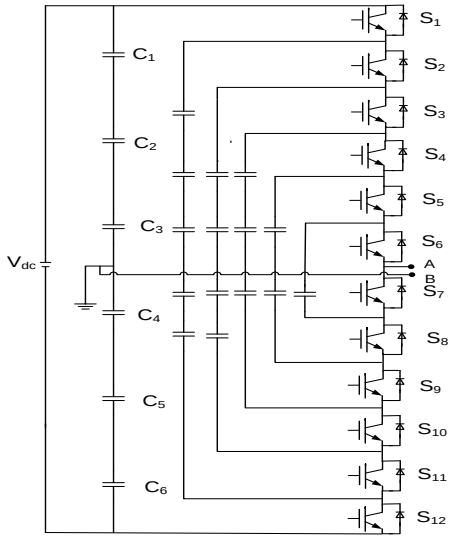


Figure 5: Single-phase 7-levelFlying-capacitor MLI.

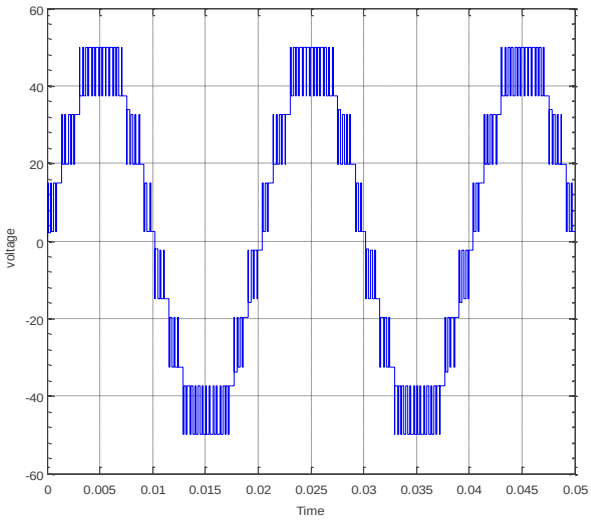


Figure 6: Output phase voltage waveform of 7-level Flying-capacitor MLI.

III. PROPOSED TOPOLOGY

Asymmetrical dual bridge MLDCLI is one of the most important topology in the family of multilevel inverter (MLI). It requires least number of component compare to cascade H--bridge multilevel inverter and symmetrical dual bridge dc-link inverter. It consist two cell of H-bridge, first H-bridge work to increase the level of the dc-link voltage and second H-bridge provide bi-directional power flow through the load. Each cell has built to four switches and an connected auxiliary switch is series with dc source, combination shunted through an anti parallel diode. In this topology switch is used IGBT.DC voltage source are consider to be identical since all of them are either batteries, solar cell, etc. it has two separate dc source and different voltage. Asymmetrical seven level dual bridge dc-link multilevel inverter can operates in different modes witch are given.

When switch S1, S2,S7 and S8 turned ON, an output voltage is V0 obtained with diode D1 working as forward-bias. When switches S1, S2, S6, S8 and S9 are turned ON, an output voltage isV1 obtained with diode D1 working as reversed bias. When switch S1, S2, S7,S8 and S9 are turned ON, an output voltage is V0+V1 obtained with D1 working as reversed-bias.

When switch S1, S2, S6 and S8 are turned ON, an output voltage is "zero" obtained for "zero" level with diode D1 working as forward-bias. When switch S3, S4, S7andS8 are turned ON, an output voltage is –V0 obtained with diode D1 working as forward-bias. When switch S3, S4, S6,S8 and S9 are turned ON ,an output voltage is -V1 obtained with diode D1 working as reversed-bias. When switch S3, S4, S7,S8 and S9 are turned ON, an output voltage is – (V0+V1) obtained with diode D1working as reversed-bias.

For operation of seven level V0:V1= (50:100) V along with positive and negative cycle. The pair of switch S1 and S2 is used for positive half cycle, switch S3 and S2 is used for negative half cycle. If we take V0 = 50 = Vdc than V1= 100 =2Vdc and V0+V1 = 150 =3Vdc.Cause of asymmetrical dc voltage source decreasing the switching losses, increasing the efficiency and eliminating the resultant effects of de-rating. Asymmetrical dual bridge dc-link multilevel inverter can be expressed using the relation 2(2n+1)+1,where n is the number of voltage source excludingV0.

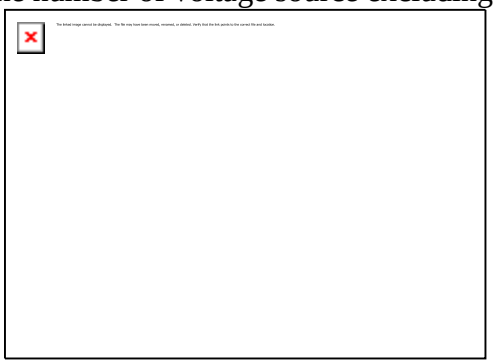


Figure 7: Single phase Asymmetrical 7-level DBMLDCI.

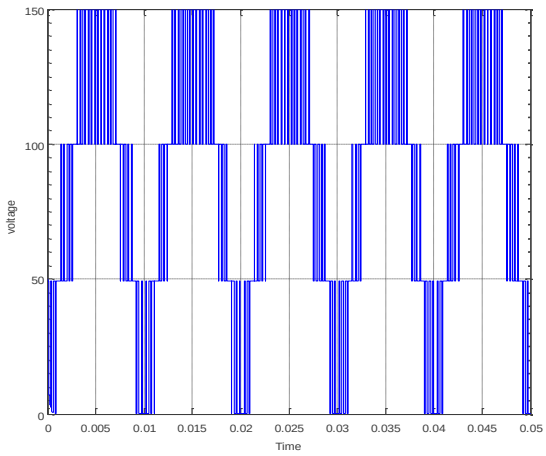


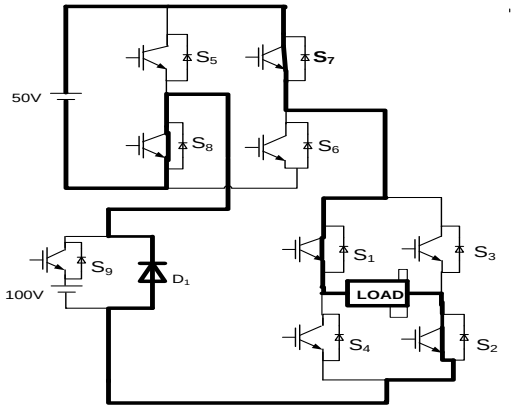
Figure 8: DC link phase voltage waveform of 7-level DBMLDCLI.

Table I Comparison in terms of power components used for different level.

Voltage level	Switching states									Output voltage
	S1	S2	S3	S4	S5	S6	S7	S8	S9	
3	1	1	0	0	0	0	1	1	1	+3V
2	1	1	0	0	0	0	0	1	1	+2V
1	1	1	0	0	0	0	1	1	0	+1V
0	1	1	0	0	0	0	0	1	0	0V
-1	0	0	1	1	0	0	1	1	0	-1V
-2	0	0	1	1	0	0	0	1	1	-2V
-3	0	0	1	1	0	0	1	1	1	-3V

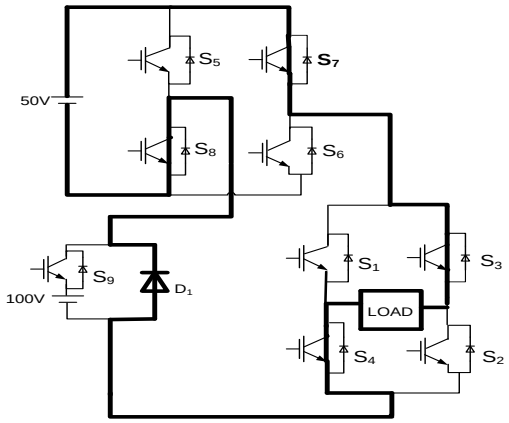
OPERATING MODES

For convenience to explain the operating modes for various levels, the dc link structure is represented by fixed dc source in the upcoming diagrams. The operation for each story of a fifteen level inverter with V0:V1 = (50:100) V along with positive and negative half cycles is explained pictorially through +3 level to -3 level. It will be seen from Figure 9. The pair S1–S2 or pair S3–S4 in the H-bridge alternately is required to take to extract the first level of the output voltage and goes through a similar sequence for other levels. The form of the output voltage shown in Figure 10 clearly indicates the devices that conduct for the various levels of the output voltage.



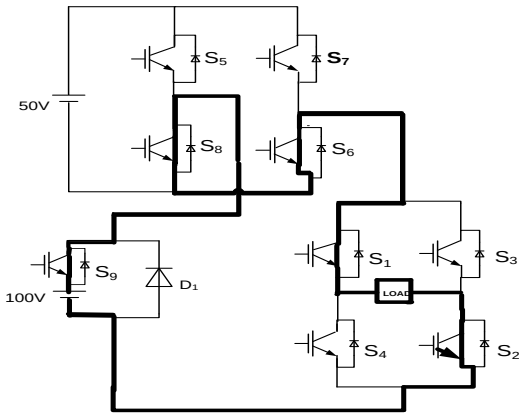
Level +1

(a)



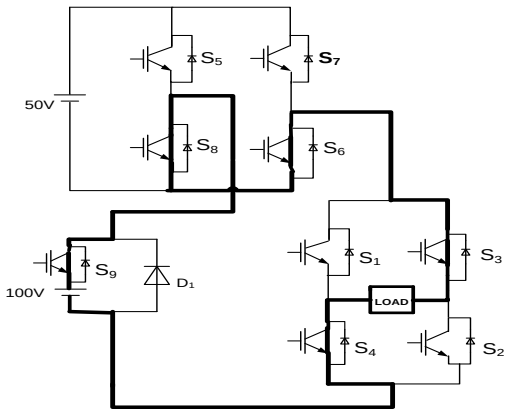
Level +1

(b)



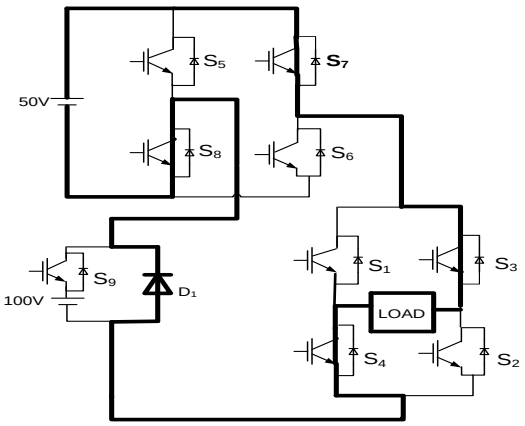
Level +2

(c)



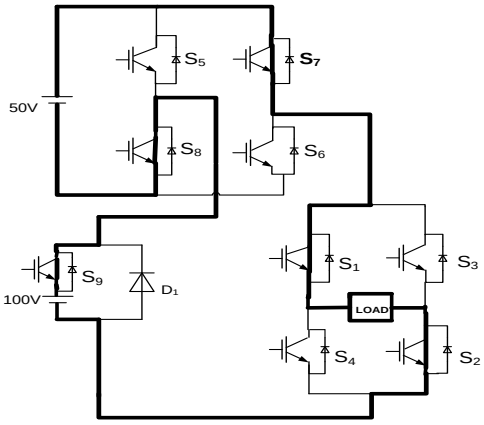
Level -2

(d)



Level +3

(e)



Level -3

(f)

Figure 9:(a) +1level ,(b) -1 level, (c) + 2level ,(d) -2 level(e), +3level, (f) -3level are operating mode for 7level DBMLDCLI.

IV. CONTROL AND MODULATION STRATEGIES

4.1. Phase opposition disposition pulse width modulation (POD PWM):-In POD PWM strategy all (N-1) carriers signal are same phase to each other above the zero-axis with same amplitude and frequency but carrier wave below zero-axis is 180^0 out of phase to above zero-axis carrier waveform.

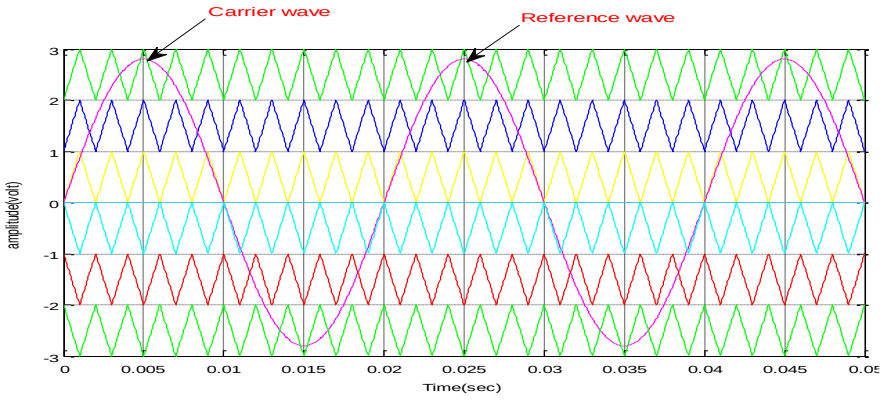


Figure 10: Carrier arrangement for POD PWM technique.

V. SIMULATION RESULT

The Figure 7 shows the proposed topology model of single-phase MLI. Table II shows its switching schemes and table I Comparison in terms of power components used for different level. The simulation parameters are as following R= 10 ohm, L= 0.01mH and DC source V1 and V2 is 50V, 100V, respectively, carrier signal frequency is 4 kHz; THD are shown in Figure12.The harmonic spectrum is carried out by using the FFT analysis in MATLAB/simulink.

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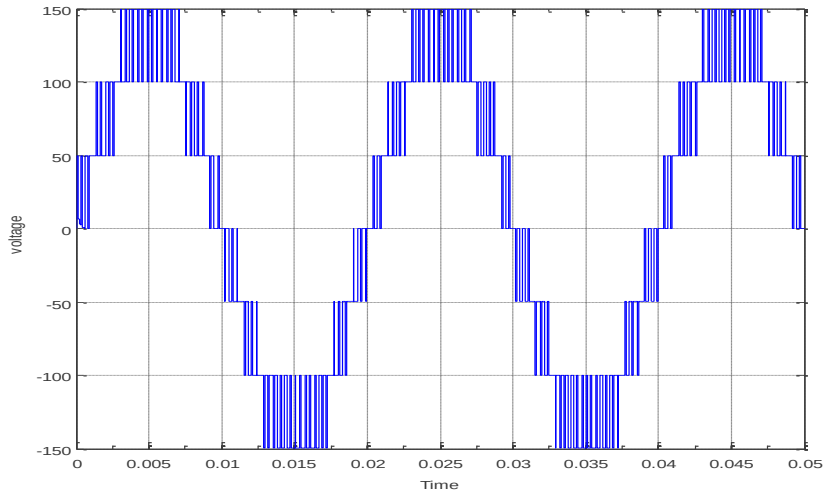

Figure 11: Output voltage waveform of 7-level Asymmetrical DBMLDCI .

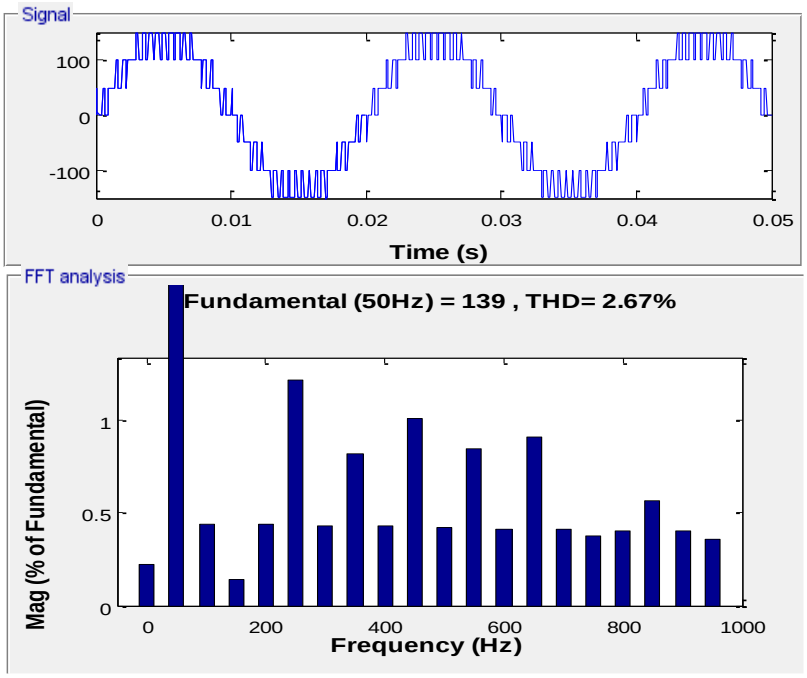

Figure 12: THD of 7-level inverter.

*TABLE-II*Comparison between topologies for 7- level inverter.

Multilevel inverter structure	Cascade H bridge	Diode clamp	Flying capacitor	Asymmetrical dual bridge MLI dc-link inverter
Main switches	12	12	12	9
Bypass diode	-	-	-	1
Clamping diodes	-	30	-	-
DC split capacitor	-	6	6	-
Clamping capacitors	-	-	15	-
DC source	3	1	1	2
Total	15	49	34	12

TABLE-III THD analysis between different PWM techniques for 7-level MLI.

PWM Technique	Modulation Index			
	1	0.9	0.8	0.75
PD PWM %THD	2.43	2.28	2.39	2.09
POD PWM %THD	2.39	3.12	2.67	2.59
APOD PWM %THD	2.48	2.46	2.55	2.42
VF PWM % THD	8.15	9.04	10.36	10.75
PS PWM %THD	2.96	2.19	2.06	2.71
CO PWM %THD	7.04	6.63	5.31	6.82

VI. CONCLUSION

An MLDCLI structure suitably built using a dual bridge configuration has been offered with a view to reduce the number of power switches to synthesize an increasing level of output voltages. The topology has been prepared using an appropriate choice of voltage ratios between the constituent parts in the power module. The acquirement of the desired results has been found to add a feather to vindicate the technology revolution in progress. The higher quality of output voltage that can be taken out using the new structure will go a long way in insinuating greater horizons of power converter interfaces in the automated world.

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