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Controlling of disturbed voltage due to the combination of linear and nonlinear load by using a DSTATCOM topology

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Abstract— DSTATCOM is one of the key FACTS Controllers. In a power distribution network, the main purpose of the DSTATCOM (distribution static compensator) is load compensation. A new modified topology for DSTATCOM applications with the nonlinear load (also linear load) and along with the non-stiff source is proposed in this paper. The proposed topology consists of two capacitors: one is in series which is along with the interfacing inductor and the other in shunt with the active filter. Due to the combination of linear and nonlinear loads the voltage profile obtained in a distribution network is somewhat disturbed. The proposed topology enables a better voltage profile than the conventional topology. Thus the desired voltage profile can be obtained with this modified topology. A simulation study using MATLAB for the proposed topology has been carried out and the results are presented.

Keywords- non-stiff source, reduced dc-link voltage, distribution static compensator (DSTATCOM), PCC, hybrid topology.

I. INTRODUCTION

Power Quality related issues are of most concern nowadays. The widespread use of electronic equipment, such as information technology equipment, power electronics such as adjustable speed drives (ASD), programmable logic controllers (PLC), energy-efficient lighting, led to a complete change of electric loads nature. These loads are simultaneously the major causers and the major victims of power quality problems. Due to their non-linearity, all these loads cause disturbances in the voltage waveform. While "power quality" is a convenient term for many, it is the quality of the voltage—rather than power or electric current—that is actually described by the term. Power is simply the flow of energy and the current demanded by a load is largely uncontrollable [1], [4].

Power quality is an issue that is becoming increasingly important to electricity consumers at all levels of usage. Active power filters have been proposed [2], to improve the quality of power. The distribution static compensator (DSTATCOM) is a FACTS device (shunt active filter), that injects currents into the point of common coupling (PCC) (the common point where source, DSTATCOM and load are connected) such that the, pf(power factor) correction, load balancing and harmonic filtering can be achieved.

Practically, the load is remote from the distribution substation and it is associated with feeder impedance. The inverter switchings distort both the source currents and the PCC voltage, due to the presence of feeder impedance. In such situations, the source is termed as non-stiff source.

The compensation performance of any active filter is decided by the dc-link capacitor voltage rating [9].Generally, the line-to-neutral voltages (peak value) have comparatively lower values than the dc-link voltage. The purpose behind this is to enhance a better compensation at the source voltage peak. The authors discussed loss of control limit and the current distortion limit, and stated that in order to obtain distortion-free compensation the dc-link voltage should not be less than (i.e. must be greater than or equal to) $\sqrt{6}$ times the phase voltage of the system [3]. The need of reactive power compensation of the active power filter is mainly responsible for the reference value of dc-bus capacitor voltage [3], [9].The value of the reference dc-bus capacitor voltage must be higher than the peak of source voltage at the PCC is the primary condition for reactive power compensation [10].

Therefore, based on their applications, many researchers have experimented with a higher value of dc capacitor voltage, due to these criteria [3], [7].

Due to the high value of dc-link capacitor, the VSI (voltage source inverter) becomes much bulky and the voltage and current rating of the switches used in the VSI needs to be designed (or rated) at higher values. This, in turn, increases the overall size and cost of the VSI. A few attempts have been made in the literature to reduce the dc-link voltage storage capacity.

In this paper, a new modified DSTATCOM topology with reduced dc-link voltage is proposed. The proposed topology uses two capacitors: one is the series capacitor along with the interfacing inductor and the other capacitor is in shunt with the active filter. The series capacitor without compromising DSTATCOM performance compensates the reactive power required by the load and also enables reduction in dc-link voltage. While the terminal voltage is maintained to desired value by the shunt capacitor in the presence of feeder impedance. The simulation studies are carried out using MATLAB, and results are presented in details in this paper.

II. CONVENTIONAL TOPOLOGY OF DSTATCOM

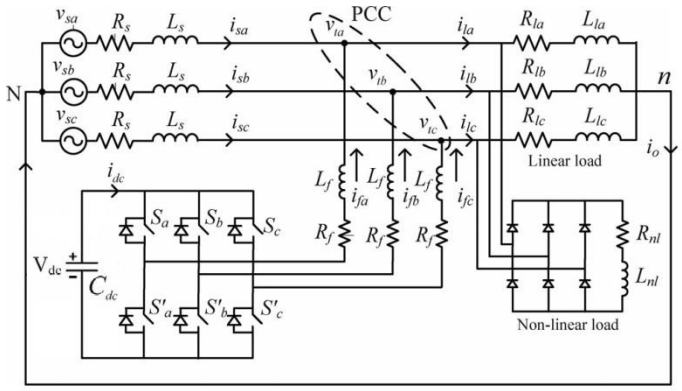

Fig.1. Equivalent circuit of the neutral clamped VSI topology-based DSTATCOM.(Conventional topology)

The conventional topology in this study is a power circuit of the neutral clamped VSI topology-based DSTATCOM is shown in Fig. 1. In this figure,a three phase voltage source is used with *vsa* , *vsb* , and *vsc* as voltages of phases *a*, *b*, and *c*, respectively. Similarly, *vta* , *vtb* , and *vtc* are the terminal voltages measured at the PCC. Also *isa* , *isb* , and *isc are* the source currents in three phases while load currents are represented by *ila* , *ilb* , and *ilc* . The shunt active filter currents are denoted by *ifa*, *ifb*, *ifc*. The feeder inductance and resistances are represented by *Ls* and *Rs*, respectively. *Lf* and *Rf* represents the interfacing inductance and resistance respectively. As shown in Fig.1, the load is the combination of both linear and nonlinear loads. *C*dc represents the dc-link capacitance and *Vdc* the voltage across it, respectively. While *i*dc is the current through the dc link.

III. PROPOSED TOPOLOGY OF DSTATCOM

The equivalent circuit of the proposed neutral clamped VSI topology-based DSTATCOM is shown in Fig. 2. The proposed topology is the combination of a capacitor *Cf* in series along with the interfacing shunt branch of the active filter and a capacitor *Csh* in shunt with the active filter in addition to the conventional DSTATCOM topology. This topology is termed as hybrid topology. The passive capacitor *Cf* has the capability to supply the required part of the reactive power to the load, and the active filter will compensate the balance reactive power and the harmonics present in the load. The dc-link voltage requirement will be significantly reduced by the adding a capacitor in series with the Lf (interfacing inductor) of the conventional topology and consequently reduces the average switching frequency of the switches. The switching frequency related components of the

Voltage Source Inverter (VSI) in the terminal voltages and source currents are largely eliminated by the shunt capacitor *Csh*. The performance of the compensator is significantly affected by the design of the shunt capacitor *Csh* and the series capacitor *Cf*. Fig. 3. shows the Single-line diagram of the proposed DSTATCOM topology.

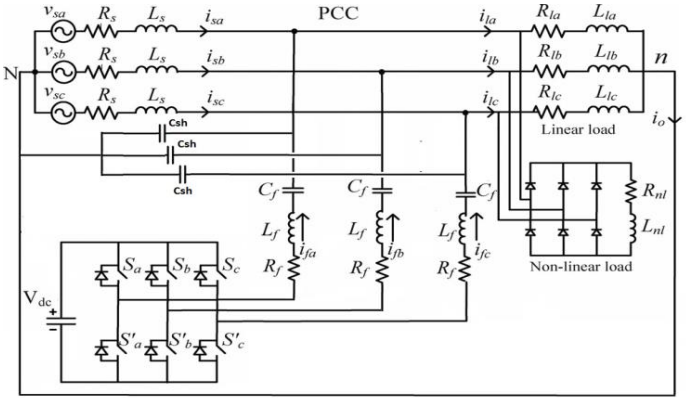

Fig. 2. Equivalent circuit of the proposed neutral clamped VSI topology-based DSTATCOM (hybrid filter).

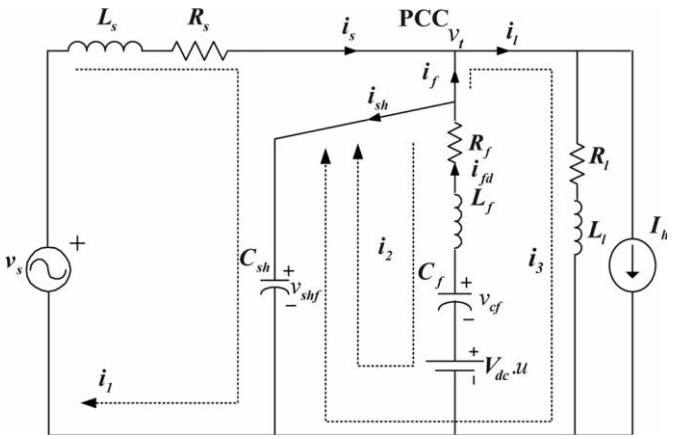

Fig. 3. Single-line diagram of the proposed DSTATCOM

IV. DESIGNING THE VSI PARAMETERS

To achieve good steady state and dynamic performance a proper design of the voltage source is very essential. The important parameters of VSIs are the values of dc storage capacitor, interfacing inductance and switching frequency of the power device. These parameters need to be designed carefully for better tracking performance. A detailed procedure of the design of the VSI parameters is given in [5]. The value of the dc-link capacitor is given by:

$$Cdc = \frac{(2X - X/2)nT}{(1.8Vm)^2 - (1.4Vm)^2} \quad (1)$$

Where *Vm* is nothing but the peak value of the source voltage, *n i*s the number of cycles, *T* is the time period of each cycle *and X* is the kVA rating of the systems. For example, consider a 10kVA system, i.e. *X*=10 and system peak voltage *Vm* =325 V, *n*=1/2, *T*=0.02sc. The value of *Cdc* computed is 2218μF.[5] The interfacing inductance is given by;

$$Lf = \frac{1.6Vm}{4hfsw\max} \quad (2)$$

Where fswmax is the maximum switching frequency of the switch, *h* is the hysteresis band.

We have considered a three-phase system with 230-V line-to-neutral voltage (i.e. 398V approx. phase-to-phase rms voltage). Let the hysteresis band *h* be 0.5 A. From (2), *Lf* (the interfacing inductance) is taken to be 26 mH. Using (1), the dc storage capacitor *Cdc* is computed and found to be 3300 μF [9]. For the conventional VSI topology the parameters of the system are mentioned in Table 1 below.

System Quantities	Values
Supply Voltage	230V(line to neutral)
System Frequency	50 Hz
Feeder Impedance	Zs= 1+j3.141Ω
Nonlinear load	Three phase full bridge rectifier load feeding a R-L load of 150 Ω-300 mH
Linear load	Zla = 34+j47.5 Ω Zlb = 81+j39.6 Ω Zlc = 31.5+j70.9 Ω
VSI parameters	Cdc =3300µF,Lf=26mH, Rf=0.1 Ω, Vdcref = 100V
PI controller gains	Kp=2,Ki=0.5

Table 1. Parameters Of The System

V. DESIGNING THE SHUNT CAPACITOR CSH FOR THE PROPOSED VSI TOPOLOGY

For a non-stiff source in the system which is due to the presence of the feeder impedance, the terminal voltages are distorted due to nonlinear load currents and unbalance. Also, the terminal voltages are contaminated with the inverter switching frequency components. A filter capacitor *Csh* , that is connected in shunt to each phase at the PCC as shown in Fig. 2, can be used to provide a low impedance path in order to remove these switching frequency components., It should be ensured that the feeder reactance *Ls* and the shunt capacitor *Csh* do not resonate at the fundamental frequency, while designing the shunt capacitor. If the filter capacitor and the feeder reactance resonate at a frequency ωr , then we get

$$Cshr = \frac{1}{\omega r^2 * Ls} \quad (3)$$

When ωr equals the fundamental frequency $\omega 0$, then the capacitance is denoted as Csho . *Csh* should not be chosen near to *Csho*, because at fundamental frequency, the resonance between the feeder reactance and shunt filter capacitor should be avoided. If *Csh* is very large, it results in high filter currents as the impedance between the PCC and ground becomes very small which will, in turn, increase the source currents, so

Csh >> *Csho* is not accepted. Thus, at a fundamental frequency of 50Hz and feeder impedance *Ls* = 0.01 H, *Csho* obtained is 1.0132mF. Hence we choose *Csh* as 2.2mF near to *Csho* .If shunt capacitive capacitor at the PCC is directly inserted it may lead to stability issues and also source currents and terminal voltages increase with the increase in the capacitance value [9].

VI. DESIGNING THE SERIES CAPACITOR Cf FOR THE PROPOSED VSI TOPOLOGY

If we chose Csh much smaller than Csho at fundamental frequency, the impedance between the PCC and ground becomes very high. Hence we neglect the fundamental filter current drawn by the shunt filter capacitor while designing the series capacitor value. The value at which the dc-link

voltage is set is an important consideration while designing the Cf. Generally, loads with only nonlinear current components are very rare, and the combination of the linear inductive and nonlinear loads contributes to the most of the electrical loads. The value to which the dc-link voltage is reduced plays a vital role in the design of the Cf.

Generally, loads with only nonlinear components of currents are very rare, and usually most of the electrical loads are combination of the linear inductive and nonlinear loads. Let Vbase be the base voltage of the system and Smax the maximum kVA rating of the system, then the minimum impedance in the system can be given as

$$Z\min = \frac{V^2 base}{S\max} \tag{4}$$

To achieve the unity pf (power factor), the required load reactive current needs to be supplied by the shunt filter current, i.e., the imaginary part of the filter current and the imaginary part of the load current should be equal. The load current and filter current in a particular phase are given as:

$$Ifilter = \frac{Vinv1 - Vt1}{Rf + jXl} \tag{5}$$

$$Iload = \frac{Vt1}{Rl + jXl} \tag{6}$$

Where Vinv1 is the line-to-neutral rms voltage of the inverter and Vt1 is the PCC voltage at the fundamental frequency, $Xlf = 2\pi fLf$, $Xl = 2\pi fLl$, $Xcf = 1/2\pi fCf$, and f is the supply frequency of fundamental voltage. Equating the imaginary parts of the equations (5) and (6) (and neglecting the interfacing resistance) gives

$$\frac{Vt1Xl}{Rl^2 + Xl^2} = \frac{Vinv1 - Vt1}{(Xlf - Xcf)^2}(Xlf - Xcf) \tag{7}$$

Generally, if the filter current (if) needs to flow from the inverter terminal to the PCC, the voltage at the inverter terminal needs to be at a higher potential than the PCC. Therefore in the conventional VSI topologies, the dc-link voltage is maintained at a higher level than the voltage at the PCC.

From [8] and [9], when the load is inductive in nature, the fundamental voltage across the capacitor adds to the inverter terminal voltage. This is because, when the load is inductive in nature, the fundamental of the filter current lags the PCC voltage by 90° for reactive power compensation, and therefore, the fundamental voltage across the capacitor again lags the fundamental filter current by 90°.Due to this, the fundamental voltage across the capacitor will be in phase opposition to the voltage at the PCC. Hence, the fundamental voltage across the capacitor adds to the inverter terminal voltage. Hence, this allows us to rate the dc-link voltage at lower value than conventional design. We may choose the reduced value of dc-link voltage, such that the LC filter in the active filter leg of each phase offers higher impedance for switching frequency components and minimum impedance to the fundamental frequency component. From the system parameters given in Table I, phase-a load impedance is chosen as Z_{min} and the dc-link voltage is chosen to be 100 V. Using equation (7), the capacitor Cf value is obtained to be 60 µF[9].

VIII. MATLAB SIMULATION

A. Simulation Model

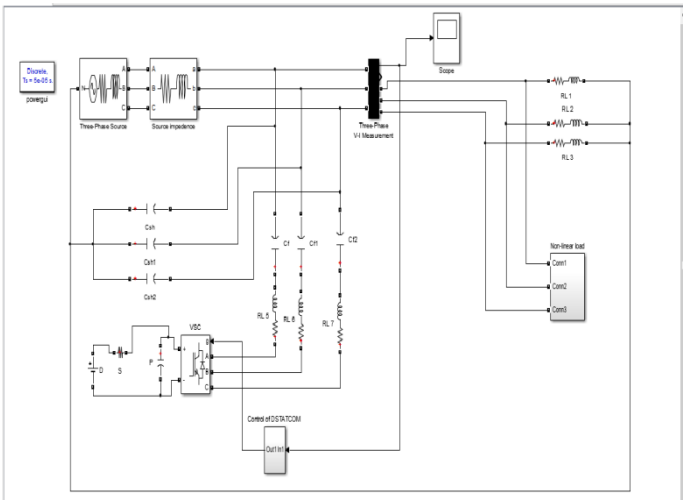

Fig .4. Matlab design for proposed DSTATCOM topology

Fig.4. shows the Matlab simulation design for the proposed hybrid DSTATCOM topology (neutral clamped VSI) in a 3-Φ power distribution system. The simulation studies for this system are performed and the results are discussed in detail in the next section.

B. Simulation Results

The simulation is carried out using simulation software MATLAB, in order to validate the proposed topology [5], [9]. The same system parameters mentioned in Table I with Cf = 60 µF and *C*sh = 2.2 mF are used in MATLAB simulation.

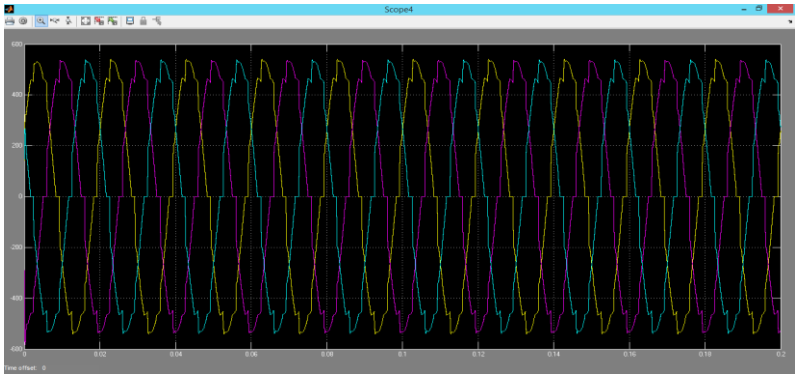

Fig. 5. Simulation results. for Terminal voltages before compensation.

For better understanding and comparison between the conventional topology and the proposed topology the topologies the simulation results for both the topologies are presented in this section. For a simple system before compensation terminal (PCC) voltages are shown in Fig. 5.

The terminal voltages are unbalanced and distorted because the load currents flow through the feeder impedance in the system. The peak-to-peak voltage of the line is around 500 V. The simulation results for the DSTATCOM using the conventional VSI topology is shown in Fig.6.

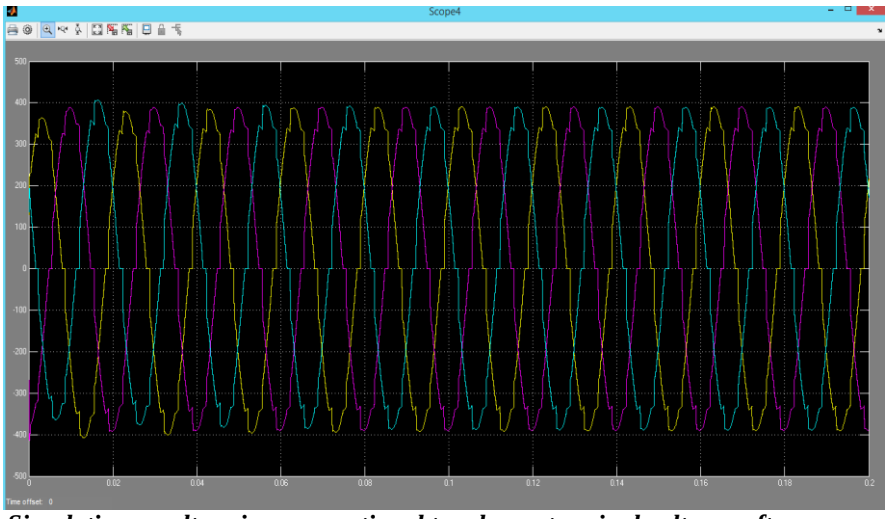

Fig. 6. Simulation results using conventional topology - terminal voltages after compensation.

Fig.6. shows the terminal voltages which contains the switching frequency components of the inverter. The peak-to-peak voltage of the line is below 400 V. The terminal voltage contains some amount of switching frequency components of the inverter.

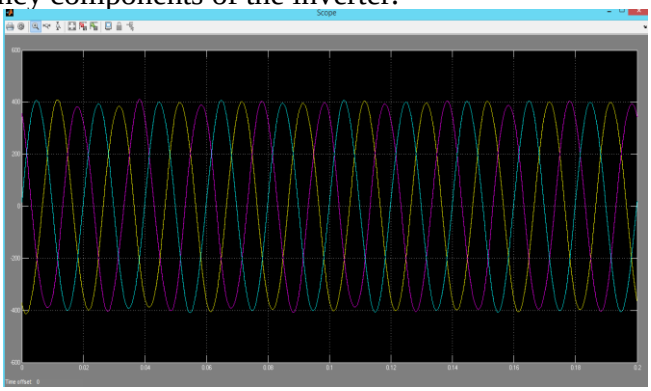

Fig. 7. Simulation results for Terminal voltages after compensation using proposed hybrid topology.

Fig.7. shows the simulation results with the proposed topology (hybrid filter). The capacitance value *Cf* in the active filter branch is chosen to be 60 µF and the reference dc-link voltages 100 V. The shunt capacitor *C*sh value is taken as 2.2 mF. From the figure, it is clear that the voltage across the capacitor and the terminal voltage are in phase opposition because the capacitor voltage ultimately adds to the dc-link voltage and injects the currents into the PCC required for the compensation.

VII. CONCLUSION

In this paper, a new modified DSTATCOM topology has been proposed which has the capability of improving the voltage profile of the power distribution network under non-stiff source and at a lower dc-link voltage. The detail explanation of the design of filter parameters is given. The proposed method is validated through simulation studies in a 3-Φ power distribution system with the neutral clamped DSTATCOM topology. Comparative studies for the conventional and proposed hybrid DSTATCOM topologies are made in detail. From this study, it is found that the proposed DSTATCOM topology has reduced dc-link voltage, less average switching frequency as compared to the conventional DSTATCOM topology.

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