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Analysis of Double-Tail Comparator with Reduced Delay

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Abstract--In Today's emerging trends low power, small chip area plays an important factor which leads to use dynamic regenerative comparators in order to increase the speed and power efficiency. Different methods were used to reduce power consumption which will reduce the delay in the circuit. An analysis on the delay and analytical expressions can also be derived for dynamic comparators. These expressions results in delay and tradeoffs. In Proposed system for low power and fast operation in small supply voltages double-tail comparator is modified by adding few transistor where the positive feedback is strengthened which will reduce delay. Clock frequency is increased to 2.5 and 1.1 GHz at supply voltages of 1.2 and 0.6 v. The standard deviation of the input-referred offset is 7.8mv at 1.2 v supply.
Keywords--Double-tail comparator, Dynamic clocked comparator, Low power design.

I. INTRODUCTION

The need for low power CMOS design has become more important for many applications specially for battery operated applications. Analog- to-digital converters (ADCs) are one of the main building blocks of most electronic devices. If the supply voltages is decreased the performance of the analog circuits will also be decreased and hence designing a low power analogue applications will be more complicated. comparator is the fundamental block in most of the ADCs with small chip area . Designing high-speed comparators is more challenging when the supply voltage is smaller.

II. RELATED WORKS

There are different techniques used for decreasing delay which includes boosting techniques, supply boosted SAR ADC design.

2.1 SUPPLY BOOSTING TECHNIQUE :

Supply boosting technique(SBT) is used for sub-micron CMOS processes. Locally supply voltage is boosted when analog signal processing. Clocked comparator can be used in SBT because the comparison of the input signals is performed in concurrent phases when voltage is stable supply boosting technique have two benefits-expansion of the input signal range, improved speed an supply voltage range and strong inversion region for all transistor operation[5]. Supply and clock are boosted during comparison period. During comparison phase the supply voltage is increased so that input signal can be increase an covering rail to rail input range. The main drawback of this technique is the capacitor used for boosting the supply voltage has to be large enough to provide adequate charge using signal processing. It also affects the device reliability due to boosting.

2.2 SUPPLY BOOSTED SAR ADC DESIGN:

This technique is based on supply boosted circuits which includes level shifter, comparator, and supporting electronics. supply boosting provides wide input common mode range and sub-1 volt operation. Source follower based level shifter,op-amps and comparators are good for SBT.

2.2.1 SUPPLY BOOSTED COMPARATOR:

Supply boosted comparator(SBC)composes of two cascade continuous time n-type differential pairs with clocked and cross-coupled comparator. First latch comparator (SBLC) uses supply boosting techniques. Second latched comparators (LC) is a regular one receiving input supply voltage. Resolution,gain of the comparator can be improved by LC.

III.SUPPLY BOOSTED SAR ADC DESIGN

Supply boosted SAR ADC design(SB)SAR ADC consist of low-voltage optimized successive approximation register logic blocks(SARL), dynamic shift registers(DSR), on-chip programmable bias generators, supply boosted comparator, clock phase generators. Two reference voltages were generated off chip to set input low level an full scale input range of the ADC. For driving analog input a low-noise off chip track and hold circuit as used. For serial data output total clock cycles 2(n+1) were required. For parallel output of SARLs could also be used for reducing conversion time to (n+1) clock cycles. In serial modes conversion speed can be increased by shifting out ADC bits faster. The drawback of this technique is robustness an static power issipation.

3.1 A COMPARATOR WITH REDUCED DELAY

In this method a conventional latch-type comparator is consisting of two cross-coupled inverters to achieve the influence against the mismatch and no-static power consumption. a new latch for low-supply-voltage operation, where the advantages of a high-impedance input, a rail-to-rail outputswing, no static power consumption, and the indirect influence of the parasitic capacitances of the input transistors (larger gate area for lower offset) to the output nodes and, therefore, to the switching speed have been kept.the is problem is the increasing gate tunnel current when the gate area is increased to develop new circuit structures that either avoid a stack of too many transistors between the supply rails, so that the technology may degrade the circuit. The determined mean delay time of the comparator which was measured with the on-chip measurement implementation will be difficult.

3.2 CLOCKED REGENERATIVE COMPARATORS

In many high speed ADCs clocked regenerative comparators found many applications.two common structures for delay time are conventional dynamic comparator and conventional dynamic double-tail comparator.

3.2.1 CONVENTIONAL DYNAMIC COMPARATOR:

ADCs uses conventional dynamic comparators with high input impedance, rail-to-rail output swing and no static power consumption. he operation of the comparator is as follows[2]. During the reset phase when CLK=0andMtail is off, reset transistors (M7–M8)pull both output nodes Outnand Outpto VDDto define a start condition and to have a valid logical level during reset. when CLK=VDD, transistors M7 andM8 are off, andMtail is on. Output voltages (Outp,Outn), which had been pre-charged toVDD, start to discharge with differentdischarging rates depending on the corresponding input voltage.

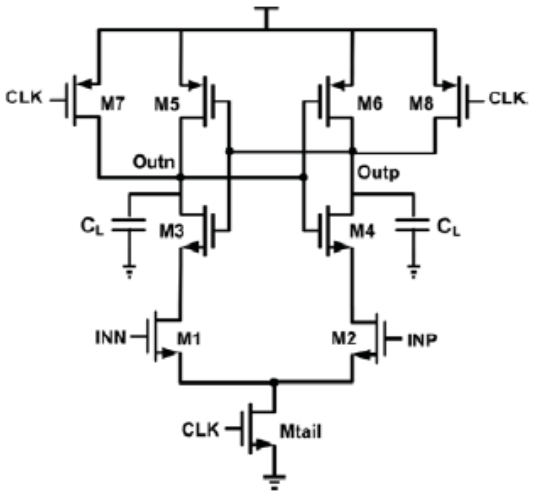


Figure. 1. Schematic diagram of conventional dynamic comparator.

Due to high impedance ,no static power consumption the parasitic capacitances of input transistors do not affected directly by parasitic capacitaqnces of input transistors.
Drawback of this system is due to stacked transistor power consumption required will be very high for proper delay.

3.2.2 CONVENTIONAL DOUBLE-TAIL COMPARATOR

This technology has less number of stacking when compared to the previous comparator design.double tail enables small current in the input stage , for low offset, large current in the latching stage. This comparator consist of two main parts, capacitive charge of load capacitance and time taken for the latch .the main drawback of this system is it will influence the initial output differential voltage and latch regeneration time of the intermediate stages of transistors[3]. The operation of this comparator is as follows (see Fig. 4). During reset phase (CLK=0, Mtail1,andMtail2 are off), transistors M3-M4 pre-charge fn and fp nodes toVDD,which in turn causes transistors MR1andMR2to discharge the output nodes to ground. During decision-making phase(CLK = VDD, Mtail1 and Mtail2 turn on), M3-M4 turn off and voltages at nodes fn and fp start to drop with the rate defined by IMtail1/Cfn(p)and on top of this, an input-dependent differential volage.

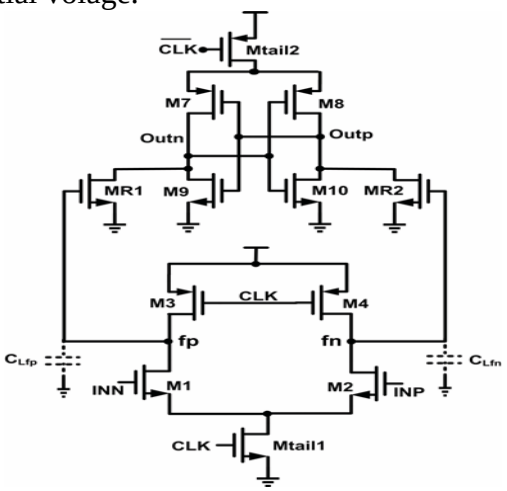


Figure 2. Schematic diagram of conventional Double-Tail dynamic comparator.

IV. PROPOSED SYSTEM

Inorder to over come the above techniques proposed technique is introduced to reduce latch time capacitive charge.

4.1 Proposed Double-Tail Dynamic Comparator:

This system is based on the double-tail comparator to increase the latch regeneration speed . delay analysis can be done by the effect of enhancing output voltage difference,increasing latch effective transconductance and reducing the energy per comparison[1]. The two factors must be considered for designing this comparator they are

4.1.1 Mismatch analysis:

Mismatch is divided by the gain from input to the output.
1.Threshold voltage mismatch
2.Current-factor mismatch

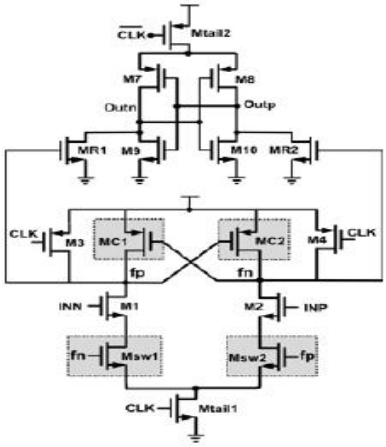


Figure. 3. Proposed dynamic comparator.

4.1.2 Kick Back Noise

Parasitic capacitances of the transistor,to the input of the comparators are coupled on the regeneration nodes when the input voltage is distributed the accuracy of the converter may decreases ,this disturbance is called as “kickback noise.”
Thus it is possible to find the size of the transistors and enhance the speed of the transistors by reducing the kickback noise.

4.2. Modified Dynamic Comparator

Drawback of proposed comparator ,the nodes f_p & f_n starts to drop with different rates according to input voltages the falling of f_n leads to ON the transistor MC_1 ON and f_p node back to VDD.node f_n to be discharged completely MC_2 OFF.

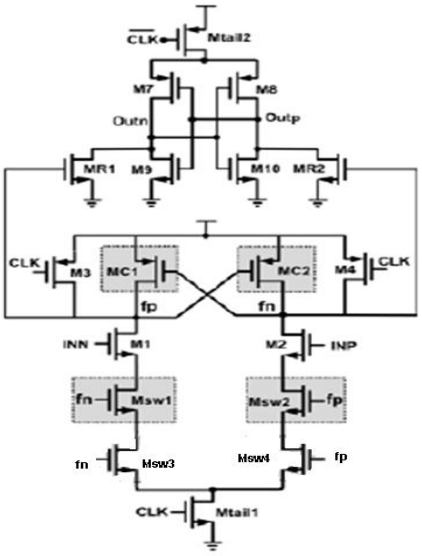
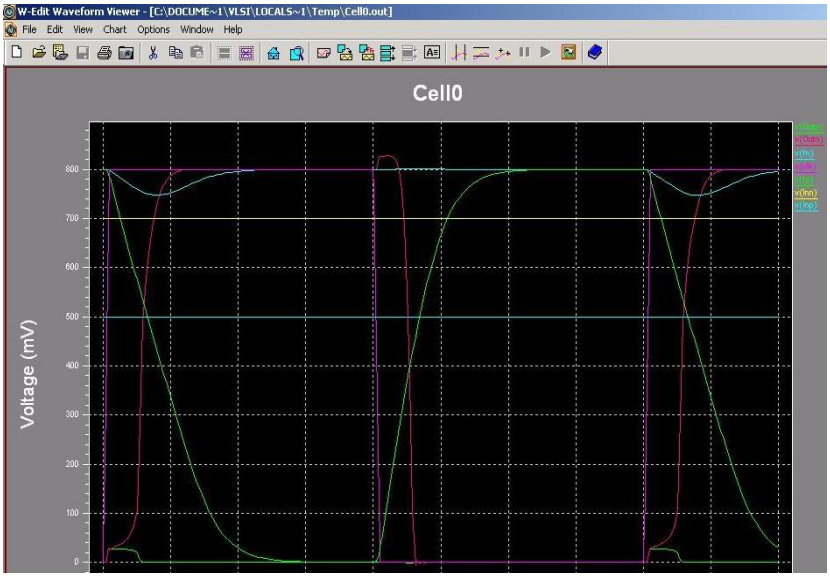
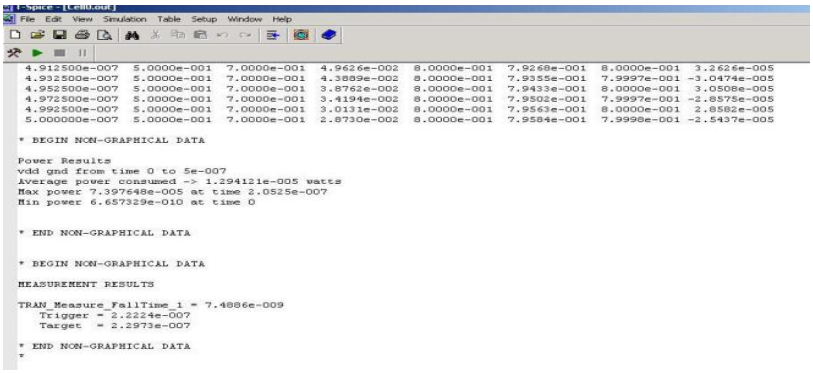


Figure.4. Modified dynamic comparator

If one of the control transistor MC_1 ON a current from VDD is drawn to ground via the input and tail transistorwill increase static power consumption.to avoid this two more switching transistor MSW_3 and MSW_4 have been added to msw1 ans msw2 in series manner thus the modified comparator will reduce the delay and power.

4.2 Simulated Results





V.CONCLUSION

In this paper , we presented a delay analysis the proposed comparator has shown a good tradeoff between delay, offset, and speed. Also ,based on theoretical analyses, a new dynamic comparator with low power,low voltage was introduced to improve the performance of the comparator.this technique provides a greater improvement in delay when compared to the conventional dynamic comparator and double-tail comprator.

REFERENCES

[1] A. Mesgarani, M. N. Alam, F. Z. Nelson, and S. U. Ay, "Supply boosting technique for designing very low-voltage mixed-signal circuits in standard CMOS," in Proc. IEEE Int. Midwest Symp. Circuits Syst. Dig. Tech. Papers, Aug. 2010, pp. 893–896.

[2] B. Goll and H. Zimmermann, "A comparator with reduced delay time in 65-nm CMOS for supply voltages down to 0.65,"IEEE Trans. Circuits Syst. II, Exp. Briefs, vol. 56, no. 11, pp. 810–814, Nov. 2009.

[3] B. J. Blalock, "Body-driving as a Low-Voltage Analog Design Technique for CMOS technology," in Proc. IEEE Southwest Symp. Mixed-Signal Design, Feb. 2000, pp. 113–118.

[4] M. Maymandi-Nejad and M. Sachdev, "1-bit quantiser with rail to rail input range for sub-1V modulators,"IEEE Electron. Lett., vol. 39, no. 12, pp. 894–895, Jan. 2003.

[5] Samaneh Babayan-Mashhadi."Analysis And Design Of A Low-Voltage Low Power Double Tail Comparator," Student member IEEE,and Reza Lotfi,Member, IEEE Vol. 22, No. 2, February 2014.

[6] Y. Okaniwa, H. Tamura, M. Kibune, D. Yamazaki, T.-S. Cheung, J. Ogawa, N. Tzartzanis, W. W. Walker, and T. Kuroda, "A 40Gb/s CMOS clocked comparator withbandwidth modulation technique," IEEE J. Solid-State Circuits, vol. 40, no. 8, pp. 1680–1687, Aug. 2005.

