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Memory Efficient Computing Structure For Multilevel Two Dimensional Discrete Wavelet Transform

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Abstract- Power consumption and area reduction are one of the major issues in VLSI applications. The efficient realization of computational complexity for 2D DWT using convolution based generic structure. The proposed design scheme introduced a Memory efficient architecture for multilevel 2D DWT using convolution based generic structure involve line buffer size of 3(K-2) M/2, where K is filter order and M is image height. Convolution-based scheme with appropriate scheduling of multilevel decomposition have lower complexity than the lifting-based design. The proposed structure does not involve Frame buffer. Convolution based generic structure can be implement in VLSI to reduced Area Delay Product (ADP) and Energy Per Image (EPI).

Keywords- very large scale integration (VLSI), Discrete wavelet transform (DWT), convolution, Area Delay Product (ADP), Energy Per Image (EPI).

I. INTRODUCTION

The discrete wavelet transform (DWT) is widely used as a powerful tool in many applications, such as signal processing, numerical analysis, computer graphics, image compression, etc. Two-dimensional (2-D) DWT is adopted in still image or a sequence of image compression applications. 3-D DWT has been employed in applications such as video compressions and magnetic resonance image (MRI) compressions as well as noise reduction between frames of a video sequence. DWT can be classified into two categories: one is based on convolution operation and the other is based on lifting scheme. Lifting scheme has lower arithmetic complexity. But its memory saving is less when compared to convolution based scheme. Convolution based scheme has lower complexity with appropriate scheduling of multilevel decomposition compared to lifting based scheme. Lifting based architecture has difficulty of scaling the structure but it has smaller hardware amount. Convolution based architecture has easy scalability according to filter length but it require large amount of hardware. Convolution based scheme uses partitioning algorithm based on state space representation method. Lifting based scheme applies pipelining to each lifting step.

II. LIFTING BASED DISCRETE WAVELET TRANSFORM

The prediction filter of the column module reads the data from MEM2, performs column-wise DWT along alternate rows (‘HH’ and ‘LH’) and writes the data into MEM2, the update filter of the column module reads the data from MEM2 performs column wise DWT along the remaining rows, and writes the ‘LL’ data into MEM1 for higher octave computations and ‘HL’ data to external memory. This generic architectural flow and it is the backbone of exiting architecture.

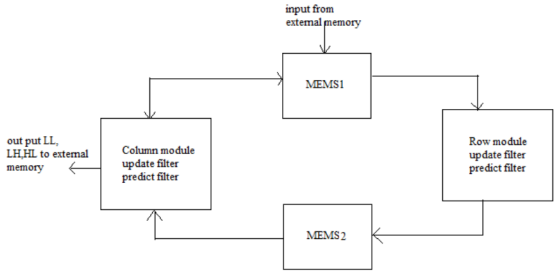

Figure 1. Lifting based architecture

Predict step even samples are multiplied by the time domain equivalent of and are added to the odd samples. In Update step the updated odd samples are multiplied by the time domain equivalent of and are added to the even samples. In Scaling step the even samples are multiplied by 1/k and odd samples by k.

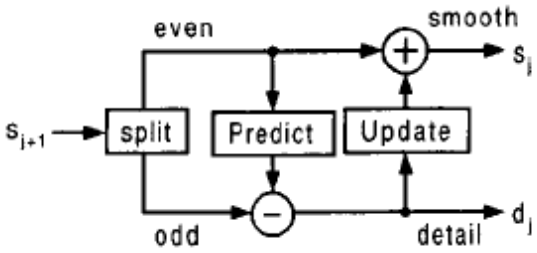

Figure 2.Lifting based implementation

III. CONVOLUTION BASED DISCRETE WAVELET TRANSFORM

The conventional DWT can be identified by convolution based execution. In this transform, the input sequences x[n] is down sampled and they are filtered by the low-pass filters h[k] and high pass filters g[k] to get the low pass and as well the high pass DWT sequence s[n] and d[n].

The row module reads the data from MEM1 performs DWT along the rows and writes the data into MEM2. The column module reads the data from MEM2 performs DWT along the columns and writes 'LL' data to MEM1 and 'LH', 'HL', 'HH' data to external memory. To replace the low and high pass filter by alternating smaller filter is lifting based architecture. In exiting convolution based architecture has easy scalability but it require large amount of hardware.

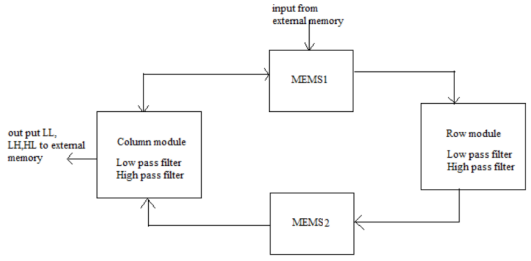

Figure 3. Convolution based architecture

IV. RELATED WORK

4.1. Recursive pyramid algorithm

Multilevel 2-D DWT can implement by using recursive pyramid algorithm . But its hardware utilization efficiency is less than 100%and it has complex control circuits. To overcome this problem folded scheme is developed.

4.2. Folded scheme

Multilevel 2-D DWT is computed by level-by-level using one filtering unit and one external unit. This design has simple control circuit and it has 100% hardware utilization efficiency. It consists of 1-D DWT and memory component. Memory component consists of frame buffer, transposition memory and temporal memory. Transposition memory makes the convolution based structure inefficient.

4.3. Parallel data access scheme

It helps to reduce the transposition memory. Memory requirement is low among all lifting based structure ·Parallel data access scheme for convolution based folded structure has less memory access.

4.4. Parallel architecture

Parallel architecture saves the frame buffer. But its input block size is sub multiple of image width. To achieve 100% hardware utilization efficiency, block size for J-level DWT is 2^{2J-1}.since block size increases with J and it involves very high hardware requirements.

V. LINE-BASED FOLDED STRUCTURE

Line-based implementations become one of the commonly used methods of VLSI implementation of 2-D DWT. It helps to achieve minimum external memory with the help of on-chip line buffer. On-chip line buffer in line-based DWT can be decomposed into data buffer and temporary buffer. The data buffer can be reduced into only few words of registers by use of a proper input data scan .So it focuses on the implementation issues of temporary buffer.

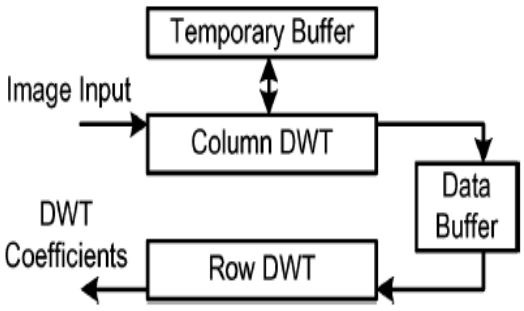

Figure 4. General line-based scheme for single-level column-row 2-D DWT

Line based folded structure helps to reduce the on-chip memory of the folded structure but it increases the complexity of the frame buffer.

VI .PARALLEL SCANNING METHOD

Parallel scanning method result in addition for two data are multiplied coefficients per cycle is saved into the on chip memory. Parallel scanning method to reduce the internal buffer size instead of the line-based scanning method.

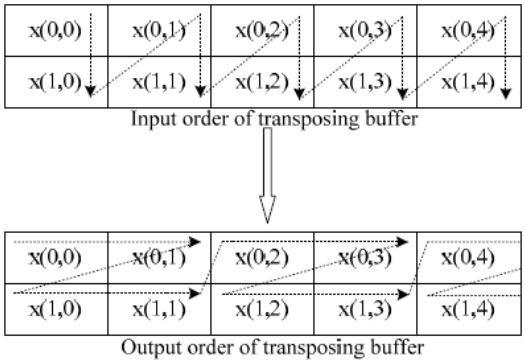

Figure 5: Input and output scanning method of transposing buffer based on parallel scanning method

VII. FOLDED DESIGN USING PARALLEL DATA-ACCESS TECHNIQUES.

Parallel data access techniques are used to avoid the transposition memory. And it introduces a complexity of frame buffer. It helps to reduce on-chip memory and increases its hardware complexity.

VIII. PROPOSED WORK

Lifting based scheme has more efficient compared to convolution due to its lower arithmetic complexity. But after analysis convolution based scheme with appropriate scheduling has lower complexity than lifting based scheme. Convolution based structure with parallel data access scheme does not involve transposition and temporal memory. It is one of the main advantages and the frame buffer can eliminate by using pipeline structure.

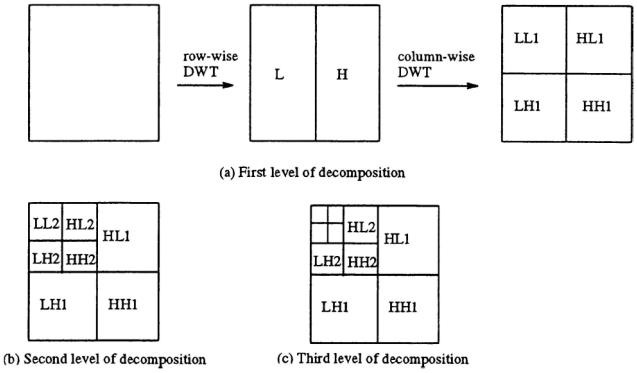

Figure 6. Three level decomposition of 2 D DWT

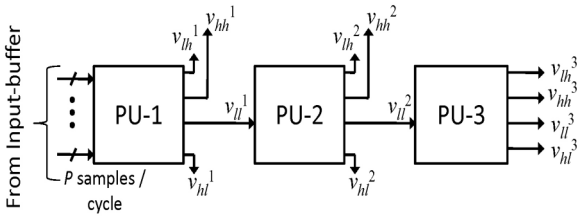

Figure 7. Proposed structure for computation of three level 2 D DWT

It consists of three processing units in order to achieve 100% hardware utilization efficiency.

Convolution based generic structure involves the following steps.

1. DWT levels are computed concurrently to avoid FB.

2. Convolution scheme is used for orthogonal as well as biorthogonal wavelet filters to derive maximum advantage of parallel data-access scheme.

3. Parallel data access is applied in each DWT level to reduce memory complexity of the overall structure.

4. Due to down-sampled filter computation, appropriate block size (*P*) need to be selected for the first level such that parallel data-access scheme could be applied to maximum possible DWT levels and 100% HUE could be achieved.

5. For resource-constrained applications, input block size (*P*) is required to be decided depending on the availability resources.
6. RPA like computation with line-based scanning is considered to compute rest of the higher DWT levels if the input block size is not sufficient.

IX. CONCLUSION

The proposed structure does not involve frame buffer and it involves line buffer of size 3(K-2) M/4 is independent of throughput rate. Convolution based generic structure involves less area complexity and less computation time when compared to others.

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