

Efficient IIR Notch FilterMs. Tuhina Dhuware¹, Prof. Gouri Morankar²¹M.Tech VLSI Design, Dept. of Electronics

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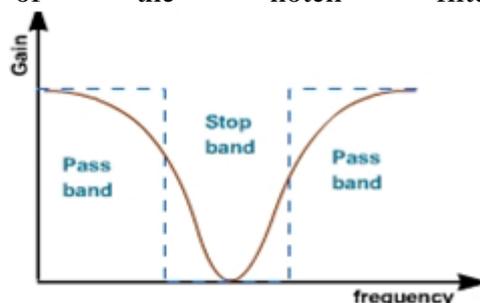
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Abstract— Speed is of chief interest in this era so IIR filters are being designed using HDL languages. The basic second order tunable notch filter is implementable using the Field Programmable Gate Array (FPGA) at 2.4 GHz. Proper pipelining with the power of decomposition-2 over the basic structure of the second order tunable notch filter has to be applied to achieve high speed. The pipelined notch filter can be implementable on virtex-5 FPGA. Parallel computing fast adders and multipliers can be used for less delay and the less power consumption. Baugh Wooly multiplier and carry select adder are to be used to achieve less delay and high speed. In order to calculate multiplier coefficients a new simpler efficient method pascal's triangle will be used.

Keywords- Pascal's triangle, Scattered look ahead pipelining, Baugh wooly multiplier.

I. INTRODUCTION

Notch filter is a band-stop filter with a narrow stopband. The work of notch filter is to attenuate, if not suppress properly, the unwanted interfering signal in present days communication (Spread Spectrum Receiver, GSM etc.) as well as non-communication receivers (Electronic Support Measure Receivers (ESM), RADAR, etc.) [1]. At the high frequency range of 2.4GHz there are so many applications ex- microwave oven, router, cordless phone, Bluetooth earpiece, baby monitor and garage opener all works on this radio frequency. Other names are 'band limit filter', 'band-elimination filter', and 'band-reject filter'. This kind of filter passes all frequencies above and below a particular range set by the component values. A *band-stop* filter works to screen out frequencies that are within a certain range and it gives easy passage only to frequencies outside of that range. A band reject (band stop) filter is a filter passes the most part of frequencies unchanged but attenuates other frequencies to very low levels in a certain range. A notch filter also known as a band stop filter with a high Q factor, i.e. it often wants to filter out the undesired signal in the specific frequency (e.g. noise) only. However, the conventional band stop filter usually has a relatively wide stop band. Response of the notch filter is as shown in



fig(1)

Fig 1. Notch Filter Response

This paper discusses about the pipelined IIR notch filter to improve its speed and performance.

II. LITERATURE SURVEY

A. Advantages of IIR over FIR filter

IIR filters have certain advantages over FIR filters. IIR filter involves feedback which helps to give accurate output. IIR filters make polyphase implementation possible whereas FIR filters cannot. IIR filters require less memory as compare to FIR filters. IIR filters are dependent on both input and output and consists of both poles and zeros whereas FIR filters have only zeros. FIR filters can only use for the linear phase applications whereas IIR filters can use for non-linear phase applications.

B. Infinite impulse response filter

Output from a digital filter is made up from previous stage inputs and previous stage outputs, which uses the operation of convolution. The difference equation for IIR filter which defines how the output signal is related to the input signal is given by

$$y[n] = \frac{1}{a_0} (b_0 x[n] + b_1 x[n - 1] + \dots + b_p x[n - p] - a_1 y[n - 1] - a_2 y[n - 2] - \dots - a_q y[n - Q])$$

where P = feed forward filter order, bi = feed forward filter coefficients, Q = the feedback filter order, ai = feedback filter coefficients, x[n] = input signal ,y[n] = output signal. An IIR filter is a recursive filter where the current output depends on previous outputs. The compressed form of the difference equation is

$$y(n) = \frac{1}{a_0} (\sum_{i=0}^P b_i x[n - i] - \sum_{j=1}^Q a_j y[n - j])$$

III. PROPOSED WORK/DESIGN METHODOLOGY

Our proposed work is based on

- Optimizing the basic second order IIR notch filter using the SLA pipelining with power of decomposition-2 and parallel processing of multiplier and adder.
- Implementation on virtex-5 FPGA for real time clock signal.

IV. PROPOSED ARCHITECTURE

The basic second order IIR notch filter structure is as shown in fig 2. Here ‘A’ represents adder, ‘M’ represents multiplier, ‘D’ represents delay, ‘X’ represents input signal and ‘Y’ represents output signal. Filter coefficients will be given to the multiplier. The proposed methodology will imply on this basic structure of the second order IIR notch filter.

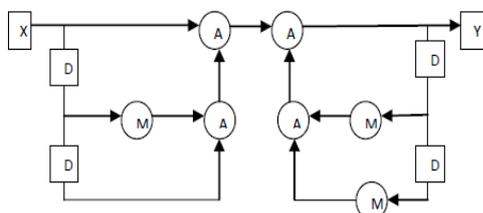


Fig 2. Second order IIR notch filter

V. PROPOSED METHODOLOGY

A. Pipelining

Pipelining leads to the reduction in the critical path which will either increase the clock speed (sampling speed) or reduces the power consumption [2]. It is a key for processors to make fast.

Fig 4. Illustrates Baugh-Wooley Multiplier which is used for both unsigned and signed number multiplication. Signed Number operands which are represented in 2's complement form. Arrangement of partial products is such that negative sign move to last step, which maximizes the regularity of the multiplication array. Baugh-Wooley Multiplier performs on signed operands with 2's complement representation to make sure that the signs of all partial products are positive [9,10].

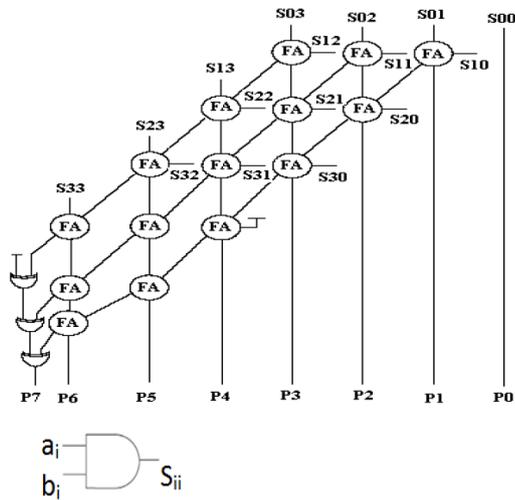


Fig 4. Block Diagram of 4*4 Baugh-Wooley Multiplier

E. Carry select adder

Adders form an almost obligatory component of every contemporary integrated circuit. The necessary condition of the adder is that it is primarily fast and secondarily efficient in terms of power consumption and chip area. There are various adder topologies present out of which we have selected a carry select adder for its low power consumption and lower delay [11]. Fig 5 illustrates the architecture of carry select adder.

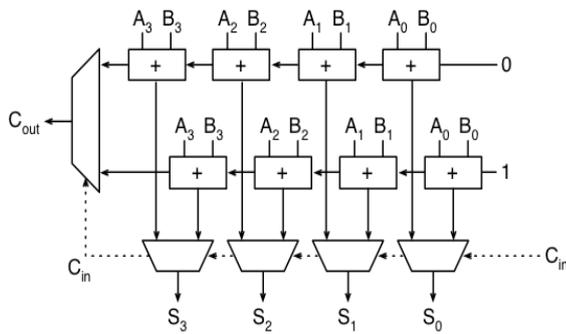


Fig 5. Carry Select Adder

F. Pascal's triangle method to calculate filter coefficients

A new and simpler approach to calculate IIR filter coefficients is pascal's triangle [1,12]. Pascal's triangle has proved very useful applications in mathematics as well as other fields. Out of such applications one wonderful application is to calculate filter coefficients of IIR filter.

VI. RESULTS OF ADDER AND MULTIPLIER

A. Baugh Wooly Multiplier

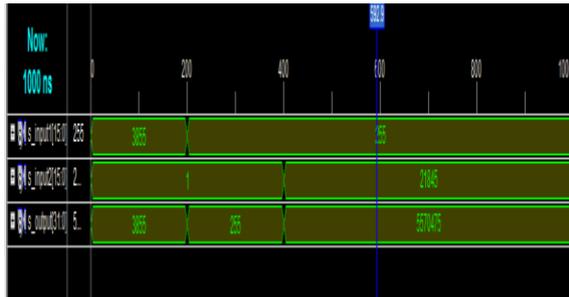


Fig 7. Xilinx ISE Simulation of Baugh Wooley Multiplier

B. Carry Select Adder

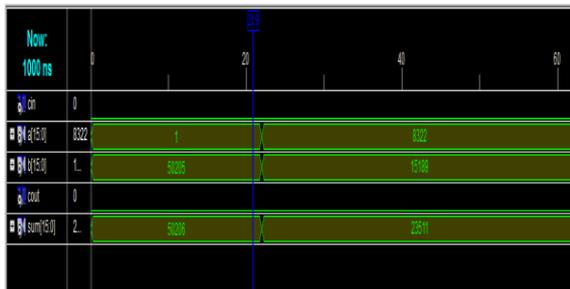


Fig 6. Xilinx ISE Simulation of carry select adder

VII. CONCLUSION

The proposed Scattered look ahead(SLA) pipelining along with the parallel processing of adders and multipliers is introduced throughout this research work. In this work second order IIR tunable notch filter can be made by using the SLA pipelining with power of decomposition 2 which will work at the frequency range of the 2.4 GHz. The proposed may be useful in communication as well as non-communication field where noise suppression is required. This can be implemented on virtex-5. The proposed work emphasis on designing of efficient tunable notch filter(low power and high speed).

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