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DESIGN OF DOUBLE PULSE TRIGGERED FLIP-FLOP BASED ON SIGNAL FEED THROUGH SCHEME

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Abstract: - In this paper double pulse triggered FF based on signal feed through scheme is proposed. Its feature solves the problem of long discharging path problem in conventional FF. Moreover, the pulse generator can be shared among many flip-flops to reduce the power dissipation and chip area. The pulse generator used here provides a narrow window to latching stage such that it reduces the pulse width thereby setup time and hold time are reduced. By this proposed feature designs better speed and power performance are achieved.

Index terms: - Flip Flop (FF), Low power, Pulse triggered, Edge triggered.

I. INTRODUCTION

In digital circuits FF are the timing elements and they impact largely on circuit speed and power consumption. Because of its single latch structure pulse triggered FF(P-FF) are ore popular than conventional type transmission gates. The primary source of power consumption in synchronous circuits are FF.

The performance of the Flip-Flop is an important element to determine the performance of the whole circuit. For example, the Clock-to-Q delay, Setup time and Hold time, all these parameters of the flip-flops can affect the performance of the whole circuit.

The demand for high-speed digital circuits at low power consumption has been increased nowadays. This is because the clock frequency been determined by system specification, the clock signal is constantly active, thus making the timing components to be more power consuming.

In the single-edge triggerd FF the output follows the input at the edge of the clock. Whereas the output takes the value of the input in dual-edge triggered FF in both the rising edge and falling edge. The output can only change at the clock edge, and if the input changes at other times, the output will be unaffected.

Thus the use of dual edge-triggered flip-flops can help to reduce the clock frequency to half that of the single edge-triggered flip-flops while maintaining the same data throughput. In other words, the dual-edge triggered flip-flop requires a lower clock frequency than the single-edge triggered flip-flop to achieve comparable performance. Therefore, the dual edge triggered flip flop offers the same data throughput of single edge-trigger flip-flops at half of the clock frequency, this thereafter translates to better performance in terms of both power dissipation and speed.

In this brief, a novel low-power double P-FF design based on a signal feed-through scheme is presented. Observing the delay discrepancy in latching data “1” and “0,” the design manages to

shorten the longer delay by feeding the input signal directly to an internal node of the latch design to speed up the data transition. This mechanism is implemented by introducing a simple pass transistor for extra signal driving. When combined with the pulse generation circuitry, it forms a new P-FF design with enhanced speed and power-delay-product (PDP) performances.

II. RELATED WORK

2.1 Explicit-Pulse Data-Close-to-Output(ep-DCO)

Due to its semi-dynamic nature it is cinsiderd to be the fastest FF. Fig.1 is the pulse generator of the Explicit-Pulse Data-Close-to-Output flip-flop. It uses the delay of three inverters to generate the pulse at the double edge of the clock. In the ep-DCO, there are two stages, the first stage is dynamic and the second stage is static. The clock pulse drives three transistors-M1,M3 and M5. The input data is connected to M2 and the circuit captures the data through M2 and its circuit is shown in Fig.2.

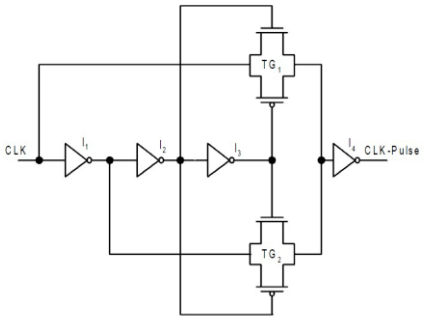

Fig.1 Circuit for Dual-pulse generation

When the flip-flop is transparent, the input data propagates to the output, after the transparent period, M3 and M5 will turn off because of the low voltage of the pulse, at the same time, point X change to the high voltage because that M1 is on at this time. So M4 is off after the transparent period. Hence, any change at the input cannot be passed to the output.

The disadvantage in this is that the internal node X will be charged or discharged at every clock cycle especially when the input data does not change, a lot of power is consumed at this point. Moreover, while the output is high, the repeated charging/discharging of node X in each clock cycle causes glitches to appear at the output. These glitches propagate to the driven gates not only to increase their switching power consumption but also to cause noise problems that may lead to system malfunctioning.

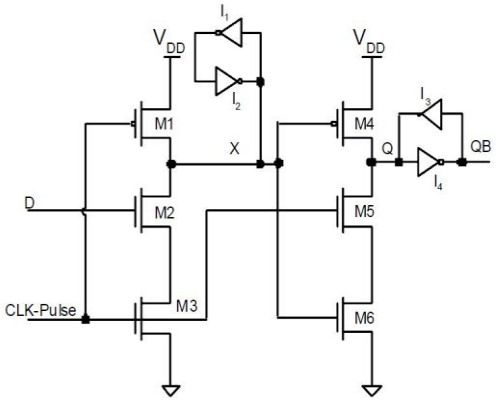

Fig.2 Explicit-pulse data-close-to-output FF

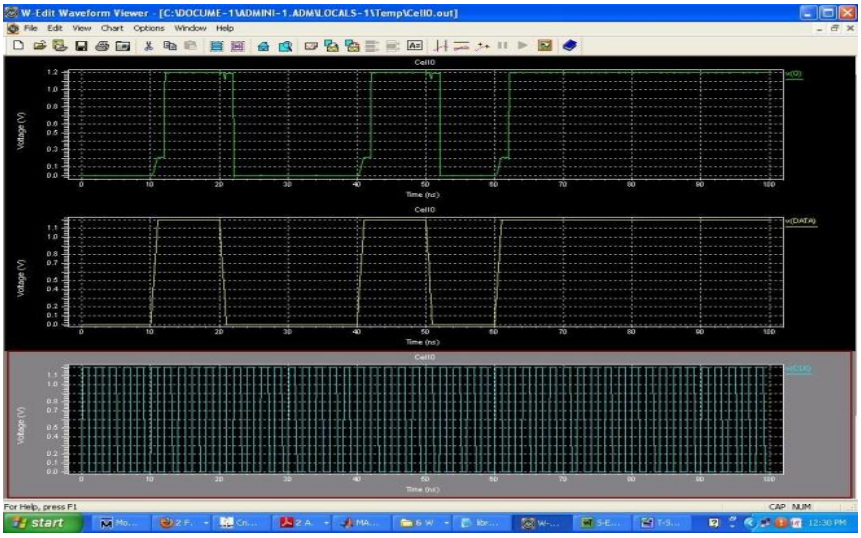

Fig.3 Output waveform of ep-DCO

2.2 Dual-Edge Triggered Sense-Amplifier FF

The schematic diagram of dual-edge triggered sense-amplifier flip-flop is presented in Fig.4. In the dual-edge triggered sense-amplifier flip-flop, there are three stages: the pulse generating stage, the sensing stage and the latching stage.

For a sense amplifier based flip-flop, when input data is high, RB will connect to Vdd and to be set to high, when input data is low, SB will connect to Vdd and to be set to high.

When pulse is high, RB will follow D and SB will follow DB, this structure can help reduce discharging time. When SB is low, output Q will be high, when RB is low, QB will be high.

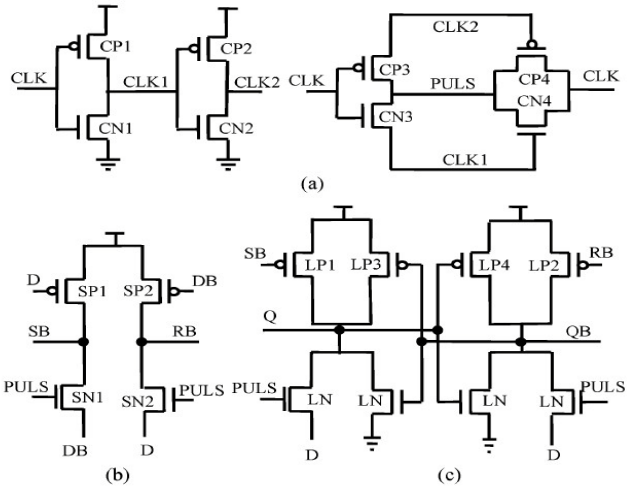

Fig.4 Dual edge-triggered sense-amplifier FF:(a) dual pulse generator (b) sensing stage (c) symmetric latch.

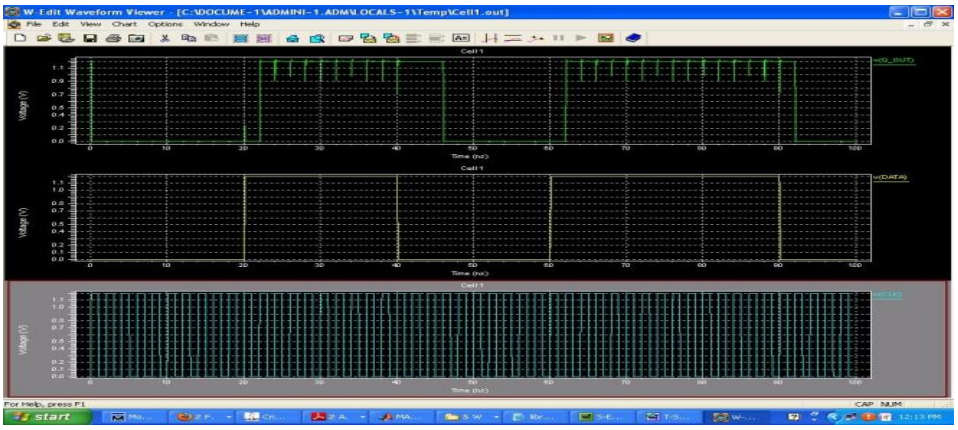

Fig.5 Output of Dual-Edge Triggered Sense-Amplifier FF

In this latching stage, there are two pulse-controlled NMOS pass transistor, these two transistors can let D and DB feed to Q and QB directly. This is the advantage of this structure. Because under the help of D and DB, Q and QB can get to high voltage of low voltage quicker, this can help decrease the Clock-to-Q delay of the flip-flop.

The disadvantage is that in the sensing stage of the flip-flop, when there is no pulse fed by the pulse generator and input data D is high, point SB will be floating, if the frequency of the clock is very low and D remains high for n cycles, the charges stored in point SB will leak out and SB will drop down from high voltage to low voltage, in this case, the logic of the flip-flop will be wrong.

This structure of the sensing stage assumes that the frequency of the clock is very high and even if the point SB is floating, the voltage at point SB will keep high and will never drop down in this case.

2.3 Dual-Edge Triggered Static pulsed Flip-flop

Here four inverters are used in the pulse generator to obtain the delayed signals. Two NMOS transistor are controlled by the different delayed pulse and generate a narrow sampling window at both the rising edge of the clock and the falling edge of the clock. After generating the narrow pulse, the two NMOS transistor in the static latch, N1 and N2, are turned on by the pulse in a very short time. At this time, the input data can be captured by the static latch, so notes SB and RB will be charged or discharged which is determined by the input data. A smaller delay can be obtained because D and DB directly provide the signal to RB and SB respectively.

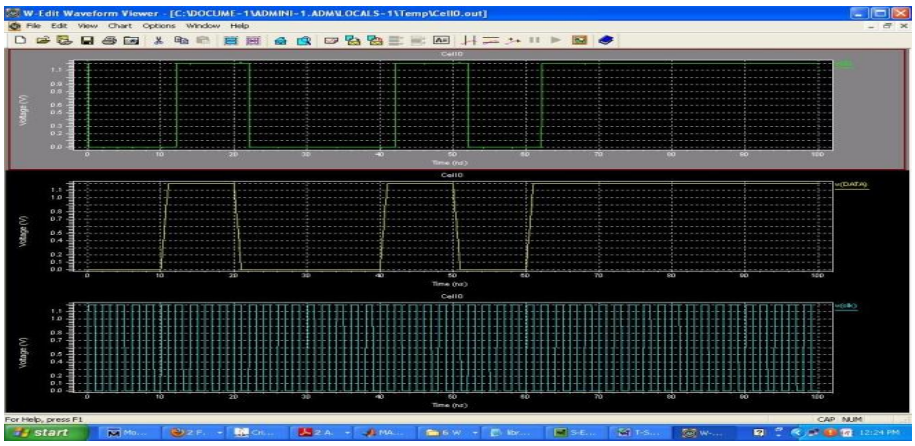

Fig.6 Output of Dual-Edge Triggered Static pulse FF

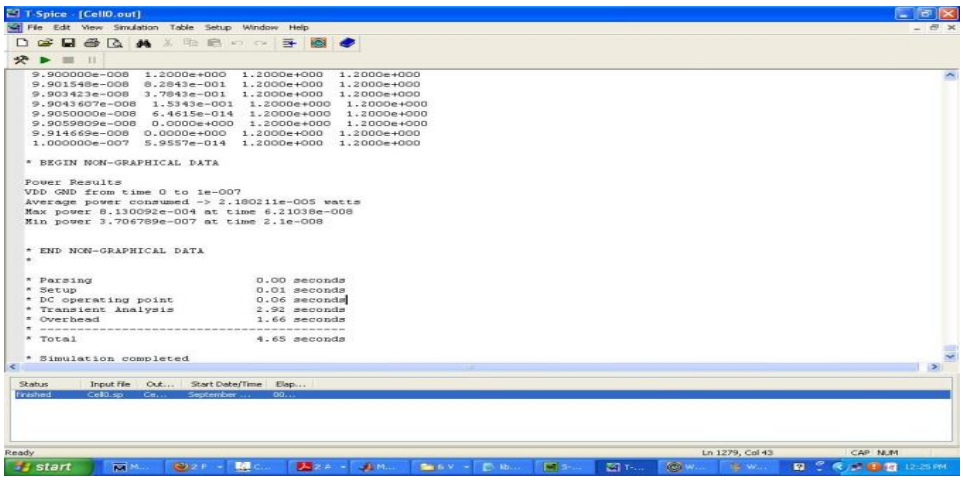

Fig.7 Power Constraints of SDFF

The disadvantages are because of capacitive loads at nodes RB and SB are very large, the flip-flop latency may be degraded. Moreover, because there is a high-voltage drop across either transistor N3 or N4 when they are off, they dual-edge triggered static pulsed flip-flop suffers from high leakage current.

III. PROPOSED WORK

3.1 Design of dual-Edge Triggered pulse Generator

This paper proposed dual-edge triggered pulsed FF with signal feed through scheme. The pulse generator designed here has two main advantages they are

1. The pulse generator can produce two narrower pulses at both rising edge and falling edge of the clock by this we can reduce the setup time and the hold time of the FF.
2. The pulse produced by the pulse generator is close to the Vdd.The working of the pulse generator is described below.

When CLK is from low to high(rising edge of the clock), because of the delay which is generated by two inverters, the voltage of CLK2 is still low and CLK3 is still high, at this time, transistor N1 is on and P1 is off because of the high voltage of the CLK, transistor P2 is on because of the low voltage of CLK2, transistor N2 is on because of the high voltage of the CLK3, so the transistors N1, N2, P1 will transfer the high voltage to the point pulse, and pulse will rise at this time. The circuit of dual edge triggered pulse generator is shown in Fig.8.

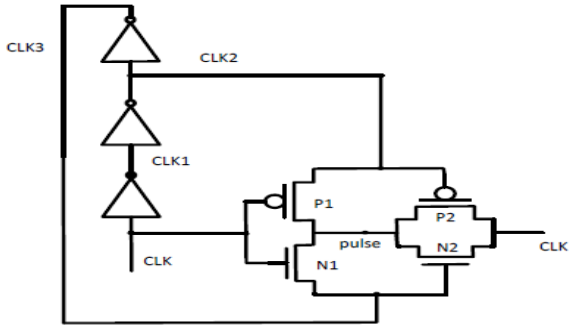

Fig.8 Dual-edge triggered pulse generator

After a very short time, the voltage of CLK2 will change to be high and the voltage of CLK3 will change to be low, transistor P1 is still off and transistor N1 is still on, but transistor P2 will turn off because of the high voltage of the CLK2, and transistor N2 will turn off because of the low voltage of CLK3, so the pulse will fall down at this time. In this very short period of time, this pulse generator generates a pulse at the rising edge of the clock. The pulse of the FF is shown in Fig.9

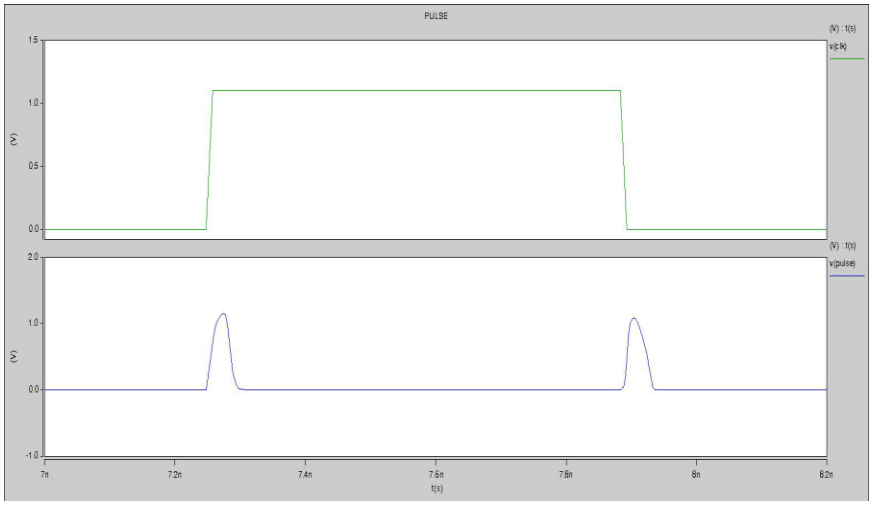

Fig.9 Pulse of the FF

3.2 Signal Feed through scheme of FF

The design of the adopted signal feed through is explained as follows. A weak pull-up pMOS transistor MP1 with gate connected to the ground is used in the first stage of the TSPC latch. This gives rise to a pseudo-nMOS logic style design, and the charge keeper circuit for the internal node *X* can be saved. In addition to the circuit simplicity, this approach also reduces the load capacitance of node *X*.

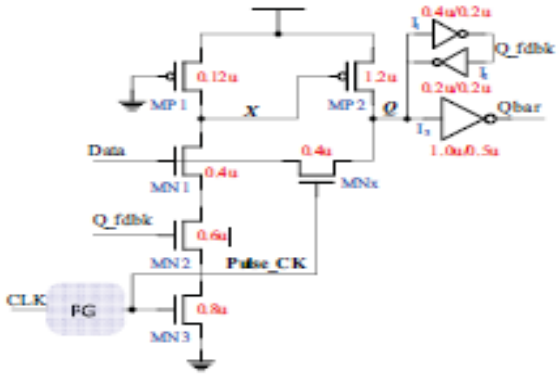

Fig.10 Circuit of proposed P-FF

Then a pass transistor MNx controlled by the pulse clock is included so that input data can drive node Q of the latch directly (the signal feed-through scheme). Along with the pull-up transistor MP2 at the second stage inverter of the TSPC latch, this extra passage facilitates auxiliary signal driving from the input source to node Q.

The node level can thus be quickly pulled up to shorten the data transition delay.The principles of FF operations of the proposed design are explained as follows.

When a clock pulse arrives, if no data transition occurs, i.e., the input data and node Q are at the same level, on current passes through the pass transistor MNx, which keeps the input stage of the FF from any driving effort. At the same time, the input data and the output feedback Q_fdbk assume complementary signal levels and the pull-down path of node *X* is off.

Therefore, no signal switching occurs in any internal nodes. On the other hand, if a "0" to "1" data transition occurs, node *X* is discharged to turn on transistor MP2, which then pulls node Q high.

In the worst case a boost is obtained from the signal feed through to the input via the pass transistor MNx thus shortening the delay.

MNx is turned on for only a short time slot, the loading effect to the input source is not significant. In particular, this discharging does not correspond to the critical path delay and calls for no transistor size tweaking to enhance the speed.

In addition, since a keeper logic is placed at node Q, the discharging duty of the input source is lifted once the state of the keeper logic is inverted.

IV. CONCLUSION

In this work, dual-edge triggered pulse generator along with signal feed through method has been implemented. And also the modified TSPC latch structure with the pass transistor incorporation in it provides a boost to the input during worst case condition. This had led to the shortening of the delay and thus we could achieve better power and speed performance in the proposed flip flop.

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