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A High Speed and Low Voltage Dynamic Comparator for ADCs

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Abstract — A new dynamic comparator is proposed and it is compared with two existing comparators in terms of voltage, delay and frequency. CMOS dynamic comparator which has dual input, dual output inverter stage suitable for high speed ADCs with low voltage and low power dissipation. A conventional comparator is replaced with dynamic comparator which reduces the delay and voltage which increases the speed. The technology scaling of MOS transistors enables low voltage and low delay which decreases the offset voltage of the comparator. The proposed system has less number of voltage and delay when compared to other comparators. The need for ultra low-power, area efficient, and high speed analog-to-digital converters is pushing toward the use of dynamic regenerative comparators to maximize speed and power efficiency.

Keywords — Analog to Digital Converter (ADC), Complementary Metal Oxide Semiconductor (CMOS), power, delay, frequency

I. INTRODUCTION

In high speed analog to digital converters the comparator design has great influence on overall performance. Comparators are the most widely used electronic components next to operational amplifiers in electronic systems. Comparators are also performed as 1-bit analog-to-digital converter and for that reason they are mostly used in large number of A/D converter. In the analog-to-digital conversion process, the first step is to sample the input. The sampled signal is then applied to a combination of comparators to determine the digital equivalent of the analog signal. The conversion speed of comparator is limited by the decision making response time of the comparator[[1].The applications of the comparators are zero-crossing detectors, peak detectors, switching power regulators, BLDC operating motors, data transmission, and others. The comparator is also known as a decision making circuit. The basic functionality of a CMOS comparator is to find out whether a signal is greater or smaller than zero or to compare an input signal with a reference signal[6]. The outputs are binary signal based on comparison. The schematic symbol and basic operation of a voltage comparator are shown in figure.1. VP is the input voltage (Pulse voltage) applied to the positive input terminal of comparator and Vn is the reference voltage (constant DC voltage) applied to the negative terminal of comparator.

Now if pulse voltage(VP), the input of the comparator is at a greater potential than the reference voltage (Vn), the reference voltage, then the output of the comparator is logic1, where as if the VP is at a potential less than the Vn, the output of the comparator is at logic 0.

If Vp > Vn , then Vo=logic1.

If Vp < Vn, then Vo=logic0.

In conventional CMOS comparator designs, the preamplifier is typically followed by a standard dynamic CMOS latch. As shown in the following subsection, this latch has a potentially large input offset and therefore requires the use of a high-gain preamplifier in order to achieve a low offset. Consequently, in high-resolution applications a single stage of 00s cannot be used, while a single-stage high-gain preamplifier with 10s suffers from a long delay. Regenerative comparators use positive feedback, similar to sense amplifiers or flip-flops, to

accomplish the comparison of the magnitude between two signals[5]. The third type of comparator emerges that is a combination of the open-loop and regenerative comparators. The combination results in comparators that are extremely fast. The comparator is also known as a decision making circuit. Voltage gain is the DC differential gain of the comparator. The output peak-to-peak swing is in the range of 3-5 V.Input offset is the voltage that must be applied to the input to get the transition between the low and the high state (same as the op-amp). The other important parameter is Response time of the comparator circuit. it is defined by the following characteristic. Response time is the time interval between the application of a step input and the time when the output reaches the respective logic level. The response time depends on the amplitude of the step input.

This paper is organized as follows: Section II describes the Comparator architecture, Section III discusses about proposed comparator circuit. Section IV discusses about the implementation of various comparators, Section V reports the most relevant measurement results and graphs. Finally Conclusions are given in Section VI.

II. PREVIOUS WORK

2.1.Conventional Comparator

Designing high-speed comparators is more challenging when the supply voltage is smaller[3]. In a given technology, to achieve high speed, larger transistors are required to compensate the reduction of supply voltage, which also means that more die area and power is needed. The dynamic comparator latch circuit is separated from the amplification branches[1]. Each stage operates independently with different clock pulses, ϕ1 and ϕ2. This separation helps the input transistors to overcome the mismatch effect inside the latch circuit before the offset of the latch circuitry is involved in the overall decision making process[13]. Hence, it significantly reduces the input referred offset voltage of the comparator.

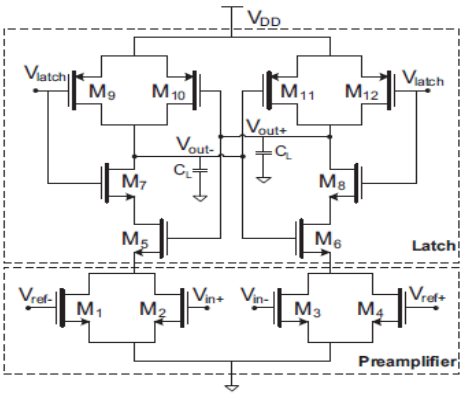


Figure.1. Conventional Comparator

2.2.Dynamic Comparator

The proposed comparator[18] works with a special three phase signaling. The signal waveform of the comparator is illustrated in Figure.3.At the first phase or pre-charging phase both ϕ1 and ϕ2 are high. Therefore, the cross coupled inverter pairs are off and pre-charge transistors discharge the output nodes to the ground. The second phase or the amplification phase will occur when ϕ1 is low and ϕ2 is still high[18].the schematic of the dynamic comparator is shown in the figure as below.

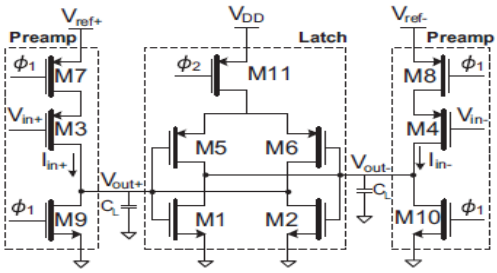


Figure.2. Dynamic Comparator

Consequently, the path to the ground is cut while the reference voltages can feed the input branch and let the input cascade transistors conduct[18]. The difference between the amount of the current produced in the input branches, I_{in+} - I_{in-} , is related to the voltage difference between the input and the reference differential voltage.

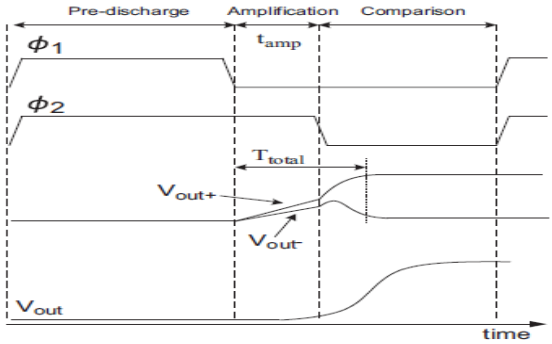


Figure.3.Conceptual Waveform

During the amplification phase, the currents set the differential voltage at the internal nodes of the cross-couple latch, Vout+ and Vout-. In the third phase, the comparison phase, the latch circuit operates and the induced differential voltage is boosted in the regenerative loop of the cross-coupled inverters.

III. PROPOSED WORK

The accuracy of comparators is mainly defined by its offset value, along with power consumption, speed has more importance in achieving overall higher performance of ADCs[11]. This can be achieved by the fully dynamic latched Comparator which is proposed in this paper. This comparator shows 14.6mV offset which is small [9] when compared to other dynamic comparators and preamplifier based comparators. This comparator not only achieves low-offset but also exhibit high-speed and low power in its operation, which can be used for low power high speed ADC applications.

In this proposed comparator we have analysed parameters such as power, frequency, delay and voltage. the frequency is analysed in tanner by taking its Rise time(RT),Fall time(FT),Low time(LT) and High time(HT).the maximum operating frequency is calculated by as given below,

Maximum Operating Frequency=1/(RT+FT+LT+HT) (Equation-4.1)
The power of this comparator is been compared with the existing comparators and total power analysis has done

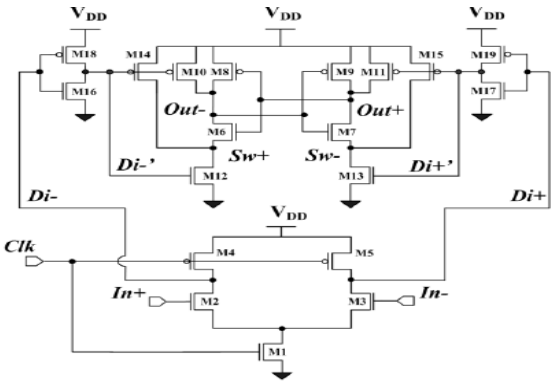


Figure.4.Proposed Dynamic Comparator

IV. IMPLEMENTATION

To compare the performances of the proposed comparator with the previous works. Each circuit here was designed using
0.25µm technology, frequency at 25MHZ is simulated at Tanner 13 version.

4.1.Conventional Comparator

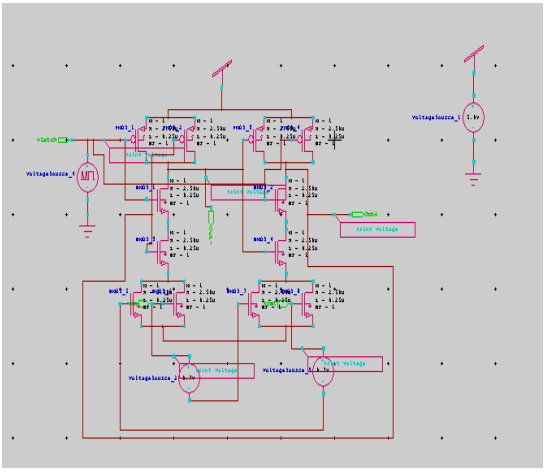


Figure.5. Schematic design of Conventional Comparator

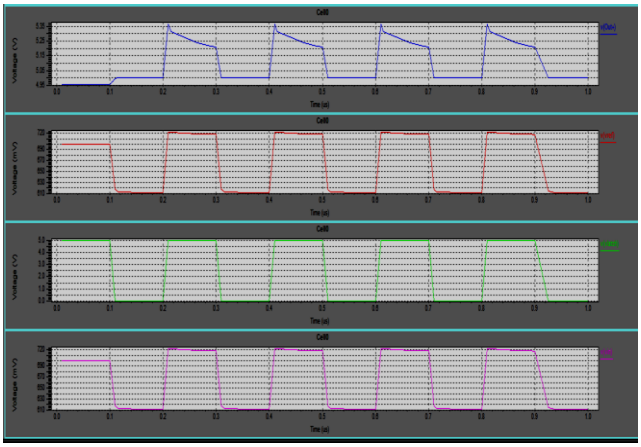


Figure.6. Transient Response of Conventional Comparator

4.2.Dynamic Comparator

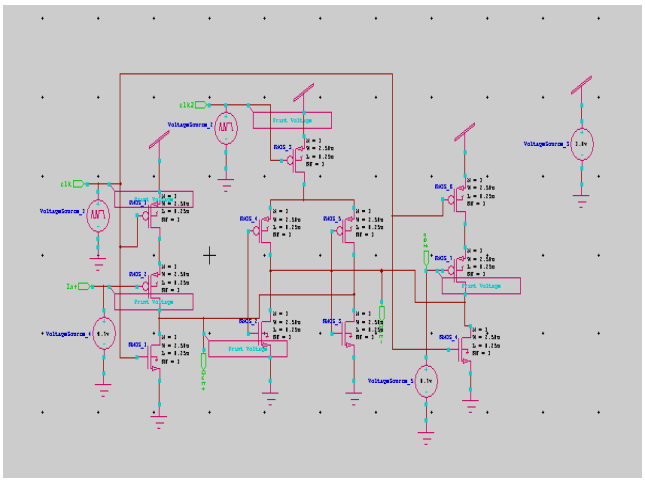


Figure.7. Schematic Design of Dynamic Comparator

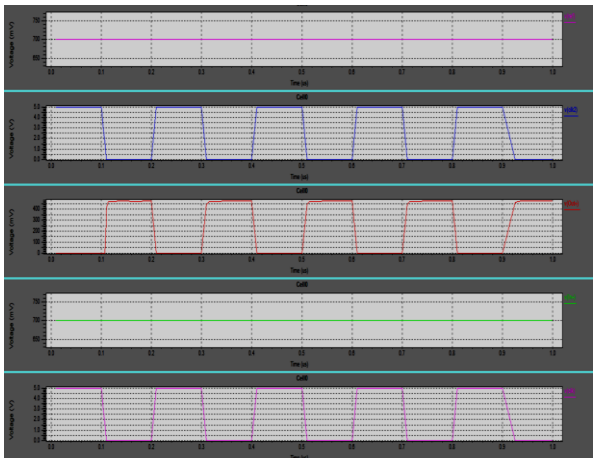


Figure.8. Transient Response of Dynamic Comparator

4.3.Proposed Dynamic Comparator

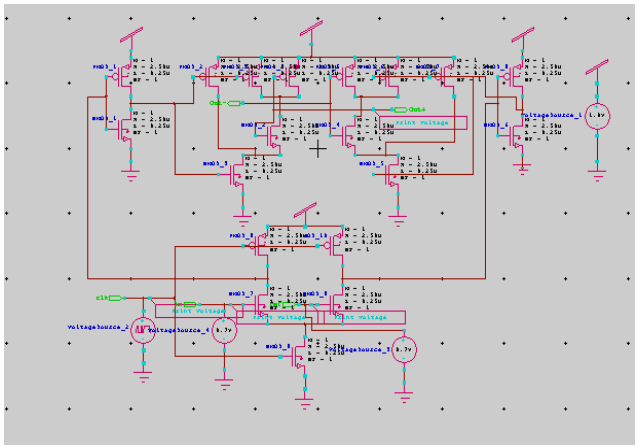


Figure.9. Schematic Design of Proposed Dynamic Comparator

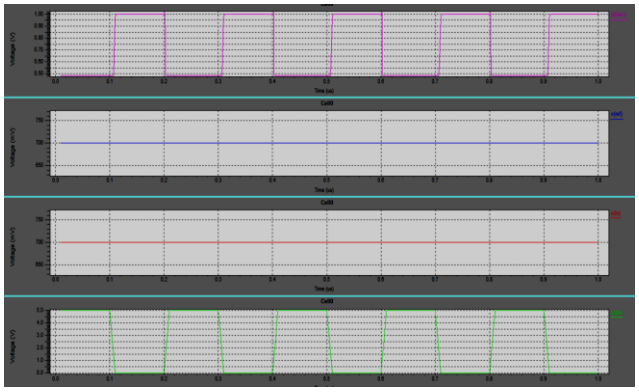


Figure. 10.Transient Response of Proposed Dynamic Comparator

V. EXPERIMENTAL RESULTS

The following table shows the various results obtained using the Tanner tool

Comparator	Number of Transistors
Existing(Comparator 1)	12
Existing(Comparator 2)	11
Proposed	**19**

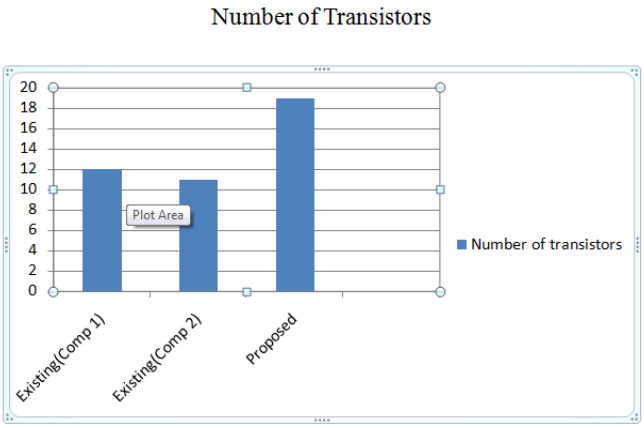
Table.1.Number of transistors used in each comparator

The following table shows voltage and delay range of various comparators.

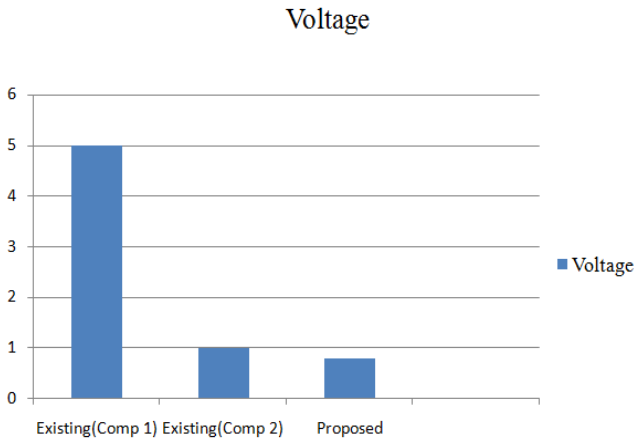
Comparator	Voltage(V)	Delay(ns)
Existing(Comparator 1)	5	10
Existing(Comparator 2)	1	8
Proposed	**0.8**	**5**

Table.2 Voltage and Delay comparisons of each comparator

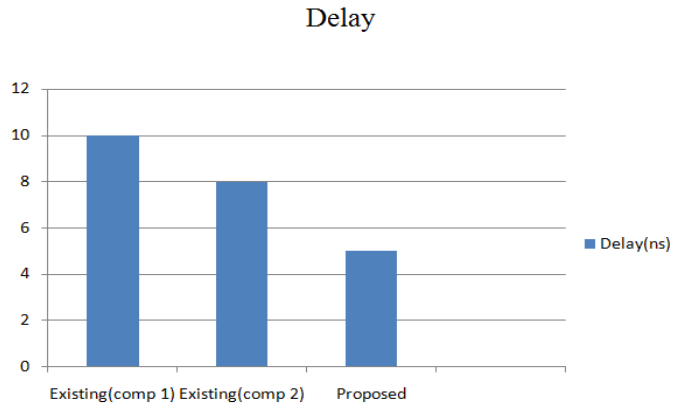
The above tables are denoted in a bar graph as follows.



This shows the bar graph for number of transistors in various comparators.



This bar graph shows the relation between the input voltage given to various comparators.



The above bar graph shows the relation between the delay obtained in various comparators. The frequency kept for all these transistors are 25MHZ.

VI. CONCLUSION

The results are simulated in Tanner with 0.25µm technology. In future, same dynamic comparator will be performed with latch load connection and offset analysis is done to remove an offset voltage due to mismatch the transistor pair. Offset voltage is removed using a common mode voltage on both the inputs. Delay will also be reduced compared with proposed dynamic comparator. The aim is to change the properties of tanner tool by which the values are changed depending on the set value.

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