Scientific Journal Impact Factor (SJIF): 1.711

e-ISSN: 2349-9745
p-ISSN: 2393-8161

International Journal of Modern Trends in Engineering and Research
www.ijmter.com

ANALYSIS OF SOLID STATE TRANSFORMER WITH PERMANENT MAGNET SYNCHRONOUS GENERATOR

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Abstract- In recent years the complexity of the grid systems has grown due to the increased penetration of renewable energy and distributed generation sources. The increased complexity requires new methods to quickly manage the changing sources and loads. This research focuses on one of such technologies, called the SST. A SST uses power electronic devices to achieve voltage conversion from one level to another. Several SST topologies have been proposed by different research groups, without a clear idea on which is most suited for grid applications.To ensure a proper choice of topology,a separate literature review is presented in this paper. The final choice of topology is extremely modular. In this, conventional dc-dc converter of solid state transformer is replaced by SEPIC converter and the analysis is done using PMSG.

Keywords-Solid StateTransformer (SST); single ended primary inductance converter (SEPIC); permanent magnet synchronous generator (PMSG); topology; voltage conversion

I. INTRODUCTION

In recent years, the complexity of the electrical grid has grown due to the increased use of renewable energy and other distributed generation sources. To cope with this complexity, new technologies are required for better control and a more reliable operation of the grid. One of such technologies is the solid-state transformer (SST). The SST technology is quite new and therefore the knowledge on the behavior of these systems in the grid is rather limited.

In the present power grids, energy is generated in large power stations and transmitted over high voltage lines. This energy is then delivered to consumers via medium and low-voltage lines. In these grid layouts, the power flow goes only in one direction: from central power stations to consumers[1]. In recent years, many European countries have started to liberalize their electricity market. This liberalization brought with it an increased penetration of renewable energy and other distributed generation sources in the grid. These developments cause the network layout and operation to become much more complex. In order to better manage future grids, sometimes also called smart grids, new technologies are required that allow better control, an increased number of power inputs and bi-directional power flow.

A key enabler for smart grids is the solid-state transformer. The SST offers ways to control the routing of electricity and provides flexible methods for interfacing distributed generation with the grid. The solid-state transformer also allows for control of the power flow, which is needed to ensure a stable and secure operation of the grid. However, this comes at the cost of a more complex and expensive system.

The advancement in semiconductor technology has provided a new alternative to the hundred year old conventional transformer technology by providing an elegant solution using Solid State Transformer. The SST is applied semiconductor technology for changing the voltage ratio. The SST can achieve high power density as well as operation at high frequency, thus reducing the size and the cost. This has provided a new opportunity for researchers, world over, to suggest new topologies, use of new material and experimentation in different environment and area of application.

A typical SST consists of an AC/DC rectifier, a DC/DC converter with high-frequency transformer and a DC/AC inverter. One of the functions of a SST is similar to that of a traditional line frequency transformer (LFT), namely increasing or decreasing the voltage. In recent years, the costs of power electronics has decreased, and more reliable, low loss, high power, high frequency power electronics have become available. The cheaper price and the fact that the solid-state transformer can replace certain grid components along with the conventional transformer, makes the solid-state transformer potentially economically feasible[2].

There is limited information available on grid behavior of the SST due to its novel technology. Simulation software allows investigation of the SST's performance without having to build a prototype first. These simulations have one major drawback, namely the long computation times. This is caused by the complexity of the control algorithms and switching elements, the simulation waveforms require long computational times to generate. The overall computation time for obtaining simulation waveforms at steady-state also drastically increase with the increased number of switching elements and control loops. The main objective is to design a single ended primary inductor converter for dc-dc conversion of the solid state transformer and to verify it under grid conditions using permanent magnet synchronous generator. By reducing the number of switching elements and control loops the overall computation time for obtaining the simulation waveforms will reduce.

II. SOLID STATE TRANSFORMER

In recent years, the interest in SST technology has increased. Several research groups are investigating the applicability of the SST for different purposes. This has led to different SST architectures and topologies.

A. Solid State Transformer Concepts

In recent years, the interest in SST technology has increased. Several research groups are investigating the applicability of the SST for different purposes. This has led to different SST architectures and topologies. The traditional Line Frequency Transformer (LFT) has been used since the introduction of AC systems for voltage conversion and isolation. The widespread use of this device has resulted in a cheap, efficient, reliable and mature technology and any increase in performance are marginal and come at great cost[5].Despite its global use, the LFT suffers from several disadvantages.

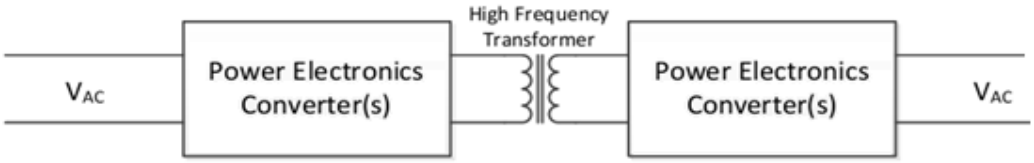

Figure 1. SST Concept

The Solid State Transformer provides an alternative to the LFT. It uses power electronics devices and a high-frequency transformer to achieve voltage conversion and isolation. It

should be noted that the SST is not a 1:1 replacement of the LFT, but rather a multi-functional device, where one of its functions is transforming one AC level to another. . Other functions and benefits of the SST which are absent in the LFT are [3][4] high controllability due to the use of power electronics ,reduced size and weight because of its high-frequency transformer.

Despite the many advantages and applications for the SST, it still faces some challenges, which keeps it from universal acceptance. These are mostly a result of the novelty of the SST technology and are expected to be resolved as the SST matures. The current disadvantages of the SST compared to the LFT can be summarized as the LFT costs less compared to the SST.

The increasing price of resources, such as copper and ferrites, to build the LFT will also have a positive effect on SST adoption. The complex nature of the SST results in a system that is unlikely to be as reliable as the LFT. However, a modular design of the SST allows for isolation and bypassing of faults. As with all systems, the reliability of the SST is expected to increase as the technology matures.

By definition, the SST consists of one or more power electronics converters and an integrated high-frequency transformer. There are several SST architectures, but based on the topologies, they can be classified in four categories [5]

1. Single-stage with no DC link
2. Two-stage with a DC link on the secondary side
3. Two-stage with a DC link on the primary side
4. Three-stage with a DC link on both the primary and secondary side

Of the four possible classifications, the three-stage architecture, with two DCs, is the most feasible because of its high flexibility and control performance. The DC links decouple the MV from the LV-side, allowing for independent reactive power control and input voltage sag ride-though. This topology also allows better control of voltages and currents on both primary and secondary side[6][7].

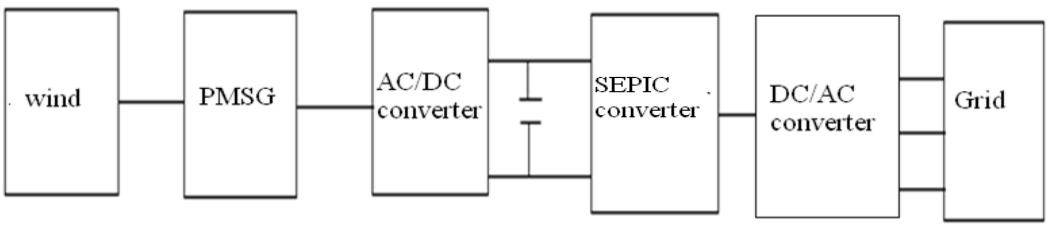

Figure 2. Block diagram

Analysis consists of a permanent magnet synchronous generator, AC-DC conversion stage , DC-DC conversion stage and a DC-AC conversion stage.AC-DC conversion stage and DC-DC conversion stage are controlled by using some kind of controllers. It is sometimes claimed that permanent magnet generator (PMG) is more expensive than double-fed induction generator (DFIG) drive trains. However, research has established that when every investment and operational factor is taken into account, PMG drive trains work out to be a cheaper, more cost-effective option over the total life cycle of the turbine. PMG drive trains actually improve efficiency over the full operational range of the turbines. Although some claim that DFIGs are more efficient than PMGs at full load generation and in high, steady winds, in reality, the efficiency of the PMG and the DFIG plus partial converter are similar when operating at 100% power. However, we know that this situation rarely occurs, and

in general working conditions, PMG drive trains have proven to be more efficient. In fact, the lower the power, the lower the efficiency of the DFIG. In addition, the Ohmic losses in the DFIG winding due to the excitation power, which are more or less constant regardless of the output, also reduce the DFIG's efficiency.

PMG has a much higher efficiency curve, and this is especially true when operating at partial power, where the highest number of operational hours is spent. As the NextWind report states: "A significant difference in power output becomes apparent when the operating speed range is taken into account. The PMG can begin producing power at very low rpms, but the DFIG is limited to a synchronous speed of less than 30%."

In terms of operational performance, using the nominal point as the benchmark leads to incorrect assumptions, as the majority of a wind turbine's lifetime is spent generating power at partial wind speeds. In effect, the lower the nominal speed of the DFIG, the poorer are its operating characteristics, mainly regarding efficiency and power factor. Due to this, DFIGs are not used in direct-drive or medium-speed turbines at all. So, the only choice for those turbines is a synchronous machine, and most often, due to poor electrical performance, DFIG cannot be used on direct-drive machines at all.

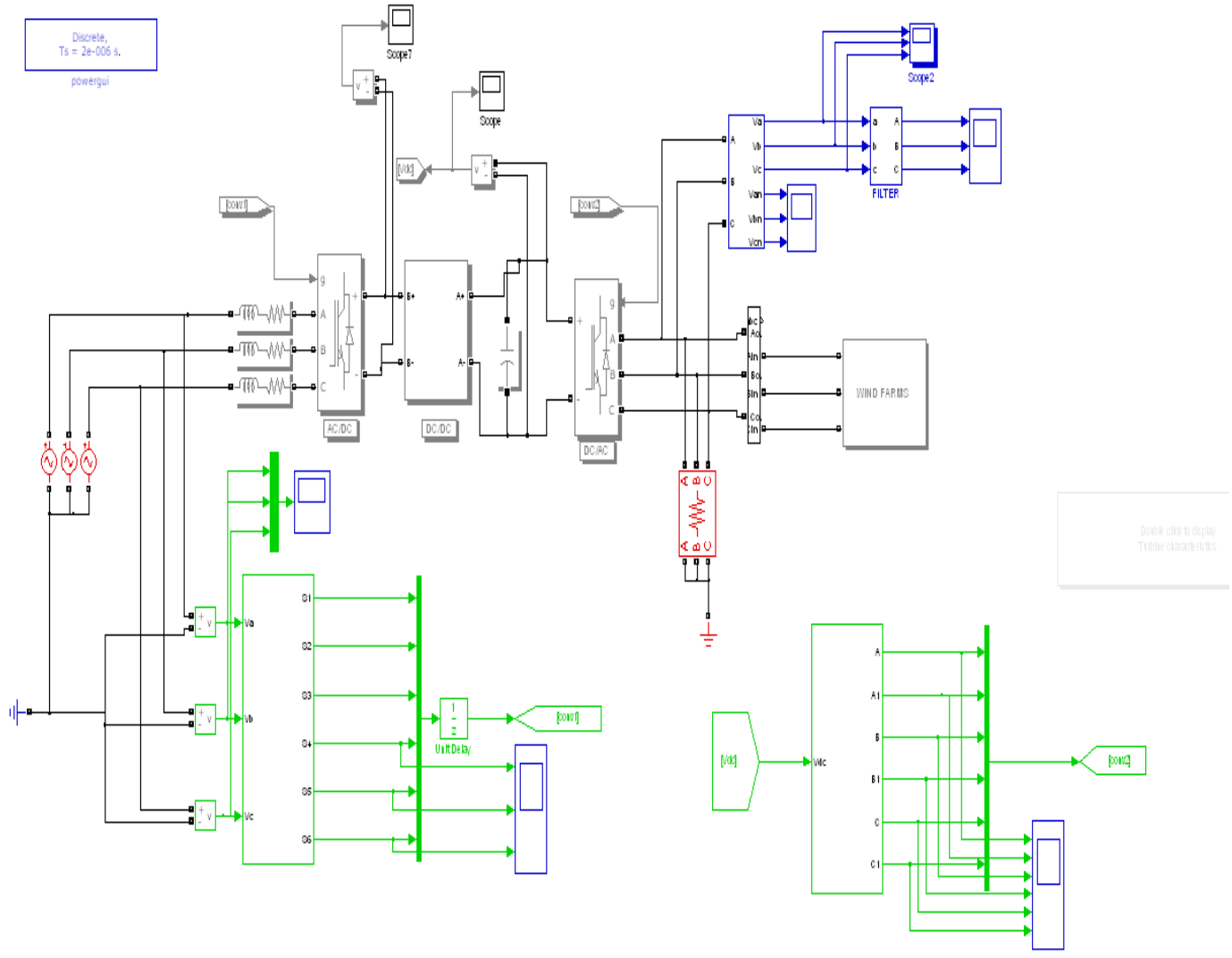

Figure 3. Simulink model of solid state transformer using single ended primary inductance converter

B. AC-DC Conversion Stage

The AC-DC conversion stage of the SST has a MV, AC-side and a DC-side.There are two options available for operating at such high voltages are two-level converters using cutting-edge high voltage power semiconductors and multilevel converters using mature power semiconductors.The use of high power semiconductor in combination with classic Two-Level Voltage Source Converter (2L-VSC) topologies has the advantage of using well-known circuit structures and control methods. However, the newer power semiconductors are more expensive and their higher power rating introduces other power-requirements and the need of HV filters.The scalability of 2L-VSCs is also an issue, since the voltage handling capabilities are restricted by the power semiconductor ratings.

Converters require multilevel modulation methods. These methods have received a lot of attention over the last years from researchers. The main reasons for the increased interest are the challenge to apply traditional modulation techniques to multilevel converters .The inherit complexities of multilevel converters due to the increased amount of power semiconductor devices. The possibility to take advantage of the extra degrees of freedom provided by the additional switching states provided by multilevel topologies.
These reasons lead to the development of several modulation methods, each with their own unique features and drawbacks, depending on the application. Depending on the domain in which the modulation technique operates, two categories can be distinguished. These are voltage based algorithms and space vector based algorithms.

Voltage Level Based Algorithms operate in the time domain. Among the several voltage level based modulation techniques, the PWM methods are the most often used. The reasons for this high adoption are high performance, simplicity, fixed switching frequency and easy digital and analog implementation[8]. Space vector based algorithms are techniques where the reference voltage is represented by a reference vector. Instead of using a phase reference in the time domain, these methods use the reference vector to compute the switching times and states. Space vector algorithms have redundant vectors, which can generate the same phase-to-neutral voltage. This feature can be used to improve inverter properties by using the redundant vector to fulfill other objectives, such as reducing the common-mode DC output voltage,reducing the effect of over modulation of output currents,improving the voltage spectrum,minimizing the switching frequency and controlling the DC-link voltage when floating cells are used. Although several space vector based algorithms are available, they are not the dominant modulation technique used in the industry. The reason for this is that carrier based PWM only requires a reference signal, carrier signals, and a simple comparator to for the gating signals.Space vector based algorithms on the other hand, require at least three stages: a stage to select the vectors for modulation, a stage to compute the duty cycle and a stage where the sequence for the vectors is generated.This means that the space vector algorithms have higher hardware requirements than the PWM techniques.

C. DC-DC Conversion Stage

The second stage of the SST is a DC-DC conversion stage. There are 5 main types of dc-dc converters. Buck converters can only reduce voltage, boost converters can only increase voltage, and buck-boost, Cúk, and SEPIC converters can increase or decrease the voltage. Single Ended Primary Inductance Converter(SEPIC) is used in this stage..This converter allows a range of dc voltage to be adjusted to maintain a constant voltage output.

D. DC-AC Conversion Stage

The third stage of the SST is an AC-DC circuit that converts the DC output from the DC-DC stage into an AC voltage. Since this stage is at low voltage, it is more feasible to use a

Two-Level Voltage Source Inverter (2L-VSC) than a multilevel inverter. The reasons for this are the cheaper, simpler circuit and the use of a more mature technology. The DC-AC conversion stage of the SST should be capable of producing a three-phase line-to-line and line-to-neutral voltage. This stage will either be connected to a low-voltage distribution grid on will work in standalone mode. In both cases, it should be capable of handling asymmetrical loads, since distribution grids are inherently asymmetrical [9]. They should also allow bidirectional power flow, to accommodate the integration of distributed generation. . Based on the required functions, the possible DC-AC topologies are three Half-Bridges Converters in parallel,three Full-Bridges Converters in parallel,three Single-Phase Three-Wire Converters in parallel,conventional Three-Phase Converter and three-Phase Four-Leg Converter.

The Continuous Pulse Width Modulation (CPWM) is an adaptation of the CPWM for three-leg inverters. The PWM signals are generated by comparing the phase-voltages and the neutral phase-voltage to a triangular carrier waveform. The simple algorithm of the CPWM allows for easy implementation with very low hardware requirements. However, compared with other modulation methods, CPWM may result in higher switching losses. The implementation of CPWM only requires the conventional abc duty cycle in order to generate the IGBT gate signals.

III. SINGLE ENDED PRIMARY INDUCTANCE CONVERTER

The single-ended primary-inductance converter is a DC/DC-converter topology that provides a positive regulated output voltage from an input voltage that varies from above to below the output voltage. This type of con-version is handy when the designer uses voltages from an unregulated input power supply such as a low-cost wall wart. Unfortunately, the SEPIC topology is difficult to understand and requires two inductors, making the power-supply footprint quite large. Recently, several inductor manufacturers began selling off-the-shelf coupled inductors in a single package at a cost only slightly higher than that of the comparable single inductor. The coupled inductor not only provides a smaller footprint but also, to get the same inductor ripple current, requires only half the inductance required for a SEPIC with two separate inductors.

Figure 4 shows a simple circuit diagram of a SEPIC converter, consisting of an input capacitor, C_{IN} an output capacitor, C_{OUT}; coupled inductors L_{1a} and L_{1b}; an AC coupling capacitor, C_p;a power FET, Q1; and a diode,D1.

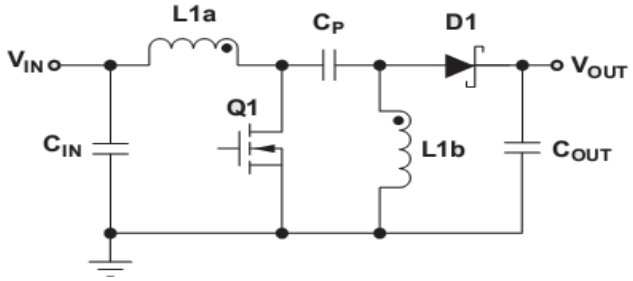

Figure 4. Simple circuit diagram of SEPIC converter

Figure 5 shows the SEPIC operating in continuous conduction mode (CCM). Q1 is on in the top circuit and off in the bottom circuit. To understand the voltages at the various circuit nodes, it is important to analyze the circuit at DC when Q1 is off and not switching.

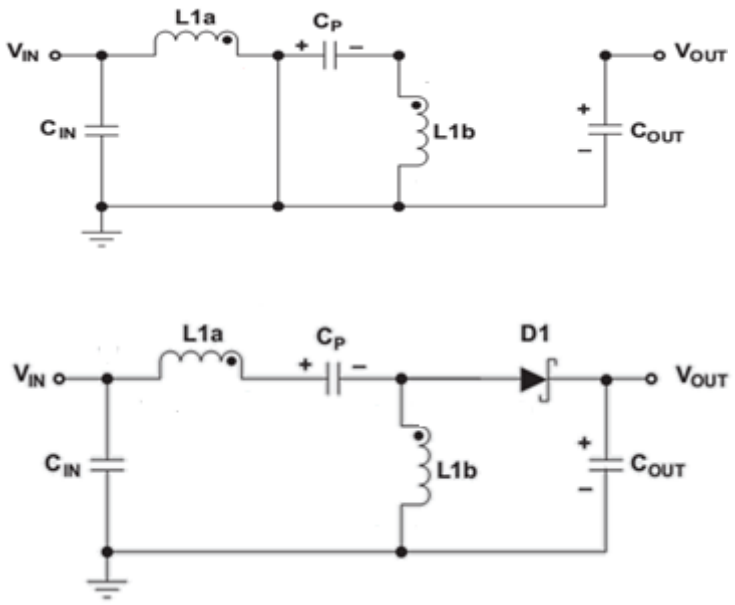

Figure 5. SEPIC during CCM operation when Q1 is on (top) and off (bottom)

During steady-state CCM, pulse-width-modulation (PWM) operation, and neglecting ripple voltage, capacitor C_P is charged to the input voltage, V_{in}.Knowing this, we can easily determine the voltages as shown in Figure 6. When Q1 is off, the voltage across L_{1b} must be V_{out}. Since C_{IN} is charged to V_{in}, the voltage across Q1 when Q1 is off is $V_{in}+V_{out}$, so the voltage across L_{1a} is V_{out}. When Q1 is on, capacitor C_P, charged to V_{in}, is connected in parallel with L_{1b}, so the voltage across L_{1b} is $-V_{in}$.

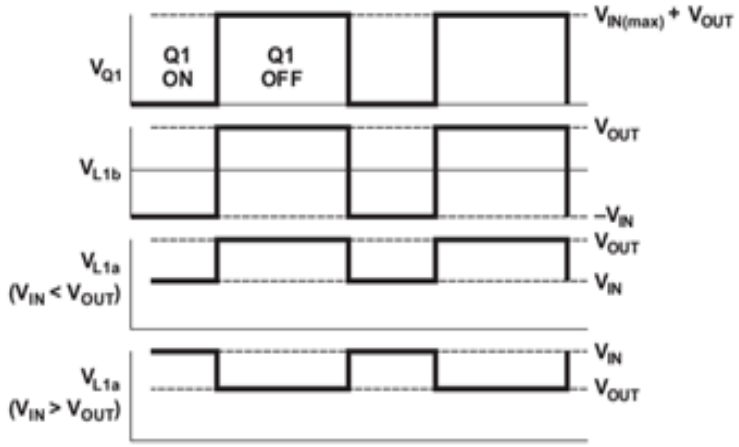

Figure 6. SEPIC component voltages during CCM

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Assuming 100% efficiency, the duty cycle, D, for a SEPIC converter operating in CCM is given by[10]

$$D = \frac{Vout + Vfwd}{Vin + Vout + Vfwd} \quad (1)$$

where V_{FWD} is the forward voltage drop of the Schottky diode.
This can be rewritten as

$$\frac{D}{1-D} = \frac{Vout + Vfwd}{Vin} = \frac{Iin}{Iout} \quad (2)$$

D(max) occurs at V_{in} (min), and D(min) occurs at V_{in}(max)

One of the first steps in designing any PWM switching regulator is to decide how much inductor ripple current, ΔI_L, to allow. Too much increases EMI, while too little may result in unstable PWM operation. A rule of thumb is to use 20 to 40% of the input current, as computed with the power-balance equation

$$\Delta I_L = 30\% \times \frac{I_{in}}{\eta} = 30\% \times I_{in}, \qquad (3)$$

In this equation, I_{IN} from Equation 2 is divided by the estimated worst-case efficiency, η, at $V_{in}(min)$ and $I_{out}(max)$ for a more accurate estimate of the input current, $I_{in'}$. In an ideal, tightly coupled inductor, with each inductor having the same number of windings on a single core, the mutual inductance forces the ripple current to be split equally between the two coupled inductors.

In a real coupled inductor, the inductors do not have equal inductance and the ripple currents will not be exactly equal. Regard less, for a desired ripple-current value, the inductance required in a coupled inductor is estimated to be half of what would be needed if there were two separate inductors, as shown in Equation 4.

$$L1a(\min) = \mathrm{L1b(min)} = \frac{1}{2} \times \frac{\mathrm{V_{IN(min)}X\ D(max)}}{\mathrm{\Delta I_L X\ f_{SW(min)}}} \qquad (4)$$

The voltage drop and switching time of diode D1 is critical to a SEPIC's reliability and efficiency. The diode's switching time needs to be extremely fast in order to not generate high voltage spikes across the inductors, which could cause damage to components. Fast conventional diodes or Schottky diodes may be used.The resistances in the inductors and the capacitors can also have large effects on the converter efficiency and ripple. Inductors with lower series resistance allow less energy to be dissipated as heat, resulting in greater efficiency (a larger portion of the input power being transferred to the load.

IV. RESULT AND DISCUSSION

The proposed work discussed above is simulated using MATLAB software and the following outputs are extracted from the simulation.

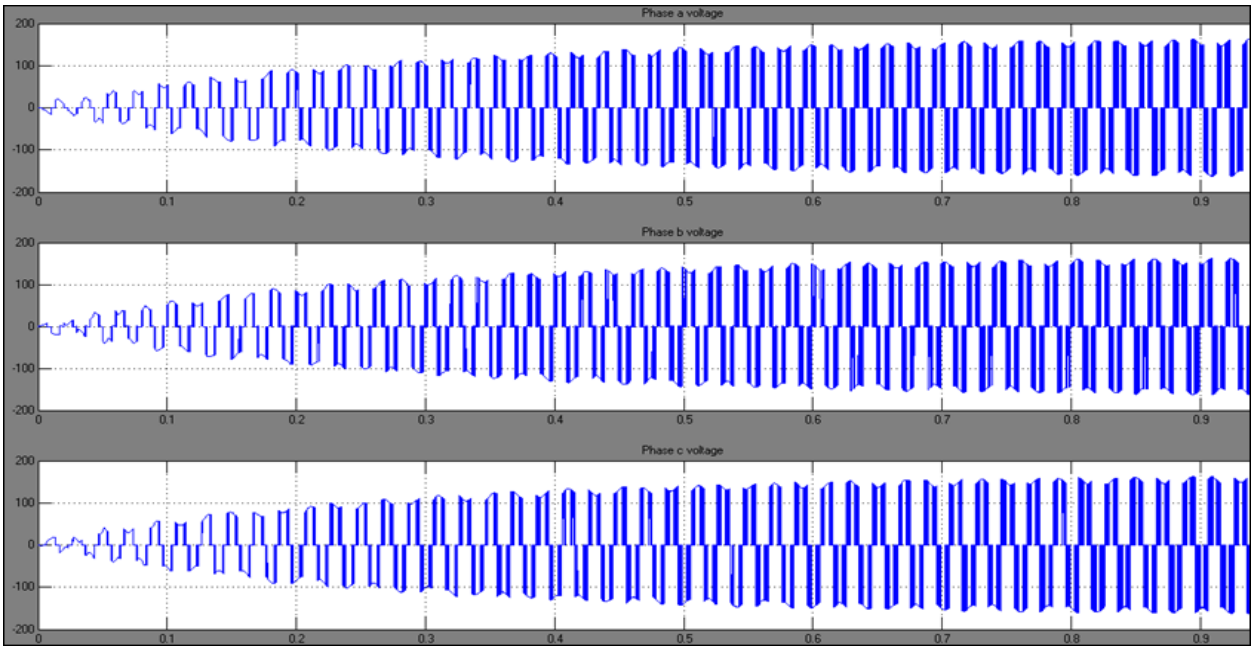

Figure 7. Output voltage of generator

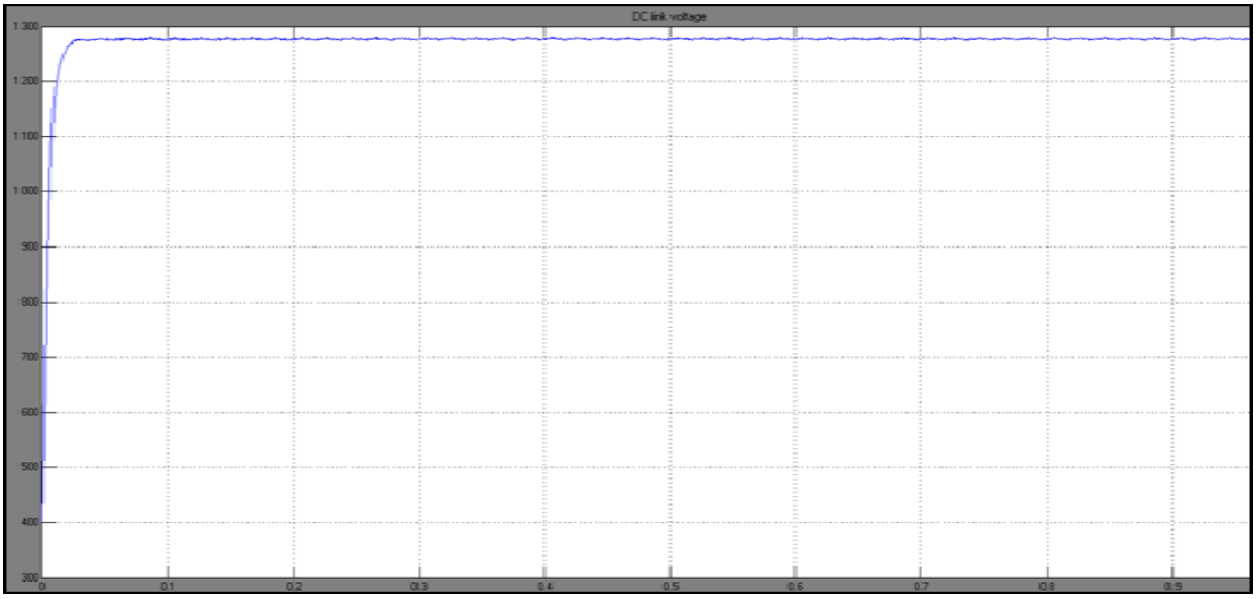

Figure 8. Output voltage of SEPIC converter

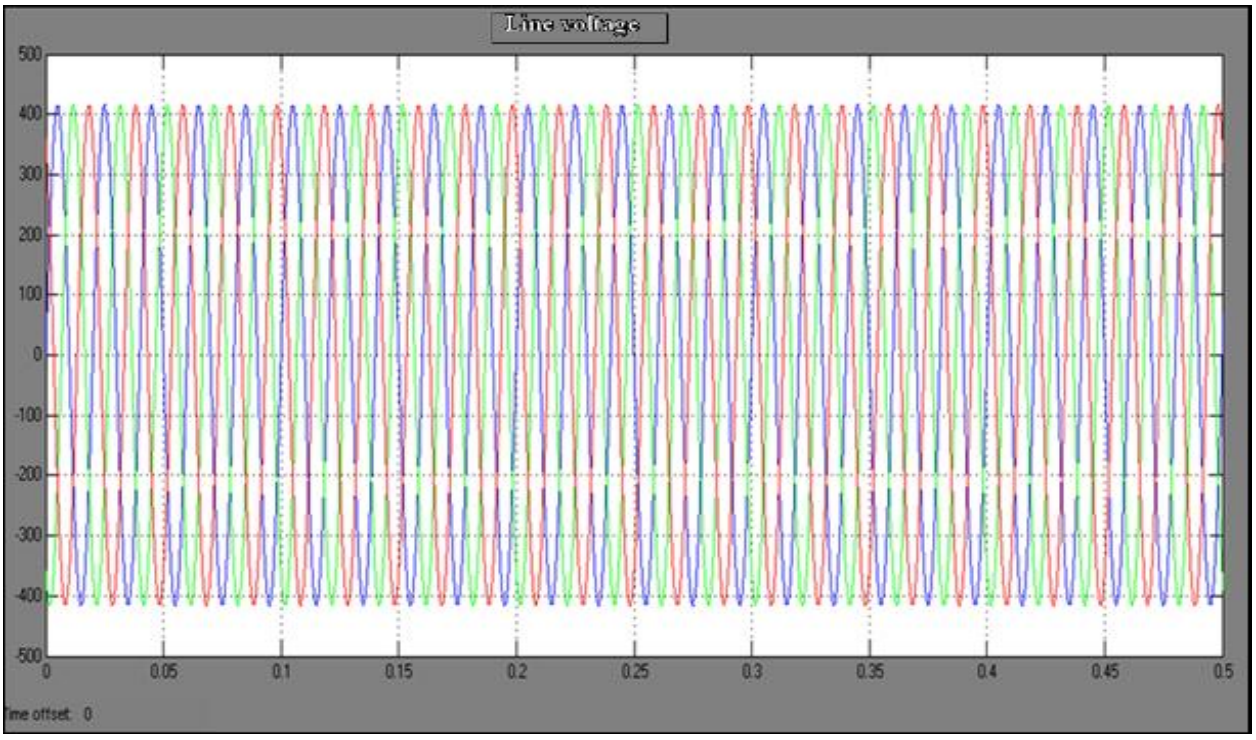

Figure 9. Output voltage of inverter

V. CONCLUSION

Energy crisis calls for a large penetration of renewable energy resources, among which wind energy is a promising one. Voltage and frequency regulation is vital to meet the grid code. Wind energy systems with integrated active power transfer, reactive power compensation, and voltage conversion capabilities has been proposed. The proposed solid state transformer was simulated using permanent magnet synchronous generator under grid conditions. Under the SST interface, the WF was rendered free of distribution power transformer and mandatory passive and active static power compensators.

Compared with the previous topology ,in this single ended primary inductor converter is used for dc-dc conversion. This reduces the number of switching elements and the computation time. There are still a lot of issues needed to be addressed, thus opening possible research opportunities. Fault operating condition is not studied yet, which is a key issue in wind energy system. Similar issues, such as how to realize the fault-ride through of the traditional wind energy system, can also be studied in the proposed SST-interfaced wind system.

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