

Analysis of Power Dissipation & Low Power VLSI Chip Design

Ms. Anshu N. Adwani¹, Mr. Hitesh V. Chopade², Prof. Swapnil S. Jain³

^{1,2} M. Tech (Electronics & Communication Engineering), DMIETR, Wardha, Maharashtra, India.

³ Asst. Professor Electronics & Telecommunication Engineering, DMIETR, Wardha, Maharashtra, India

Abstract—Low power requirement has become a principal motto in today's world of electronics industries. Power dissipation has becoming an important consideration as performance and area for VLSI Chip design. With reducing the chip size, reduced power consumption and power management on chip are the key challenges due to increased complexity. Low power chip requirement in the VLSI industry is main considerable field due to the reduction of chip dimension day by day and environmental factors. For many designs, optimization of power is important as timing due to the need to reduce package cost and extended battery life. This paper present various techniques to reduce the power requirement in various stages of CMOS designing i.e. Dynamic Power Suppression, Adiabatic Circuits, Logic Design for Low Power, Reducing Glitches, Logic Level Power Optimization, Standby Mode Leakage Suppression, Variable Body Biasing, Sleep Transistors, Dynamic Threshold MOS, Short Circuit Power Suppression.

Keywords-Low power, VLSI, CMOS, package cost, battery life, power dissipation.

I. INTRODUCTION

In modern era VLSI design efforts have focused primarily on increasing the speed to realize computationally intensive functions such as video compression, gaming & graphics etc. So, we have semiconductor ICs that successfully integrated various complex signal processing modules & graphical processing units to meet our requirement. While these solutions have addressed the real-time problem, they haven't addressed the demand for portable high speed operation, where mobile phone needs to design with all this without consuming much power. The strict limitation on total power dissipation in portable electronics applications like smart phones and tablet computers must be met by the VLSI chip designer while still meeting the computational requirements. But wireless devices are rapidly making their importance to the consumer electronics market; a key design component for portable operation namely the total power consumption of the device must be addressed. Lowering the total power consumption in these systems is important since it is desirable to maximize the run time with minimum requirements on size, battery support and required weight of batteries. So the most useful factor to consider while designing SOC for portable devices is 'low power design'.^[1]

II. PROBLEM ASSOCIATED WITH POWER DISSIPATION

Scaling of technology node increases power-density more than expected. CMOS technology beyond 65nm node arises a real challenge for any sort of voltage and frequency scaling Starting from 120nm node, each new process has obvious higher dynamic and leakage current density with minimum increase in speed. Between 90nm to 65nm the dynamic power dissipation is almost same

whereas there is ~5% higher leakage/mm² [3]. Low cost always require higher levels of integration, whereas less costly technological breakthroughs to keep power under control are getting very scarce.

III. DO WE NEED TO BOTHER WITH POWER?

Power dissipation is the main look up when it comes to Portability. The mobile device consumer keeps demanding more features and extended battery life at a lower cost. About 70% of users require longer talk-time and maximum stand-by time as primary mobile phone feature. For 3G technology we require more power efficiency, consumer also needs smaller size gadgets. It requires high levels of Silicon integration in advanced processes, where as advanced processes have inherently higher leakage current. So we must need to consider leakage current while designing low power gadgets.

IV. WHY POWER MATTERS IN SOC?^[4]

Power Management useful in System on Chip because of following concerns:

1. Packaging & Cooling costs.
2. Digital noise immunity,
3. Battery life of portable systems
4. Environmental issues.

V. SOURCES OF POWER DISSIPATION

The power dissipation in circuit is classified into three classes as described below.

1. **Dynamic power consumption:** Because of logic transitions causing logic gates to charge/discharge load capacitance.
2. **Short-circuit current:** In a CMOS logic P-branch and N-branch are momentarily shorted as logic gate changes state for short circuit power dissipation.
3. **Leakage current:** It occurs when the system is in standby mode or not powered. There are various sources of leakage current in MOSFET^[7]. Diode leakages around transistors & n-wells, Sub-threshold Leakage, Gate Leakage, Tunnel Currents etc. Increasing 20 times for each new fabrication technology.

VI. LOW-POWER DESIGN TECHNIQUES

An integrated low power methods requires optimization at all design abstraction layers as below:

1. System: Partitioning, Power lowering.
2. Algorithm: Complexity in design, Concurrency of operation, Regularity in working.
3. Architecture: Parallelism of operations, Pipelining of processes, Redundancy of data, Data Encoding & decoding.
4. Circuit Logic: Logic design Styles, Energy Recovery methods, component sizing.
5. Technology: Threshold Reduction capability, Multi Threshold Devices.

Dynamic power varies as V_{DD}^2 . So lowering the supply voltage reduces power dissipation. The selective frequency reduction technique used to lower the dynamic power requirement^[4]. At system level, multi threshold voltage can be used to reduce leakage power. For speed-up circuit and reduce power transistor resizing can be used. Sleep transistors can be used efficiently to reduce standby power. Parallel processing and pipelining can reduce power requirement. Clock disabling, power-down of selected logic blocks, adiabatic computing, software redesign to lower power dissipation are the other techniques commonly used for low power design.

VII. VLSI CIRCUIT DESIGN FOR LOW POWER

The growing market of portable gadgets (cellular phones, gaming remotes) battery-powered electronic systems require microelectronic circuits design having ultra-low power dissipation. As the integration, size, and complexity of the chips continue to increase, the difficulty in providing sufficient cooling might either add significant cost or limit the functionality of the computing systems which make use of those integrated circuits. The technology node scales down to 65nm there is not much increase in dynamic power dissipation. However the static power or leakage power is same as or exceeds the dynamic power below 65nanometer technology node.

So the methods to reduce power dissipation is not limited to dynamic power. In this paper we approaches to minimize Dynamic, Leakage power dissipation and Short Circuit power dissipation. Power minimization in a processor can be achieved at various levels of designing. So we need to optimize or reduce the power requirement of desired circuitry^[3].

Total Power dissipated in a CMOS circuit is equal to total of dynamic power, short circuit power and static power or leakage power. Designed structure for low-power requirement implies the ability to reduce all three parameters of power consumption in CMOS circuits during the designing of a low power electronic product.

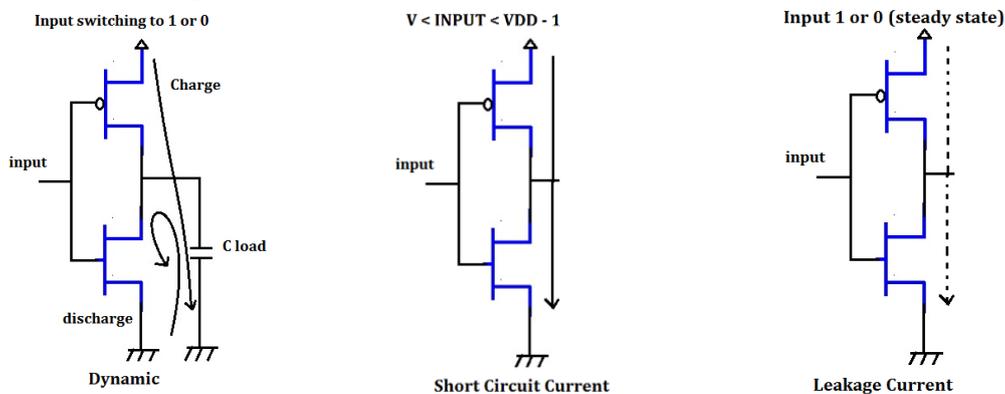


Figure 1. Components of Power in CMOS circuit $P_{total} = C_L V_{DD}^2 + t_{sc} V_{DD} I_{peak} + V_{DD} I_{leakage}$

7.1. DYNAMIC POWER SUPPRESSION

Dynamic/Switching power is due to charging and discharging of load capacitors driven by the circuit. Supply voltage variation has been the most preferred approach to power optimization, since it normally result in considerable power savings due to the quadratic dependence of switching/dynamic power $P_{Switching}$ on supply voltage V_{DD} . However limiting the supply voltage affects circuit speed which is the major short-coming of this method. So design and technological solutions must be applied to compensate the decrease in circuit performance introduced by reduced voltage. Some of the methodology often used to reduce dynamic power are described below.

7.2. ADIABATIC CIRCUITS

In adiabatic circuits instead of dissipating the power is reused. By externally limiting the length and shape of signal transitions energy spent to flip a bit can be reduced to very small values. As the diodes have thermodynamic irreversible nature they are not used in the design of Adiabatic Logic. MOSFETs should not be switched ON when there is significant potential difference between source and drain. And shouldn't be TURNOFF when there is a significant current flowing through gadget.

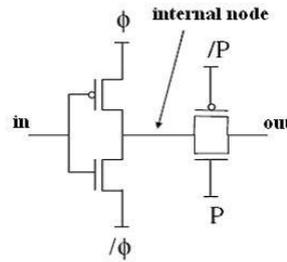


Figure 2. Charge Recovery Logic

7.3. LOGIC DESIGN FOR LOW POWER

Selection between static & dynamic topologies, conventional CMOS & pass-transistor logic styles and synchronous & asynchronous timing styles have to be made while designing a circuit. In static CMOS circuits, about 10% of total power consumption is due to short circuit current. However, in dynamic circuits there is small amount of power dissipation to reduce the sharing, as there is no direct dc path between GND & power supply.^[6]

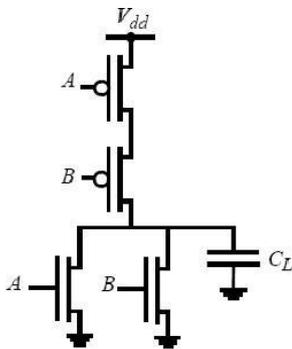


Figure 3. (a) Static NOR circuit

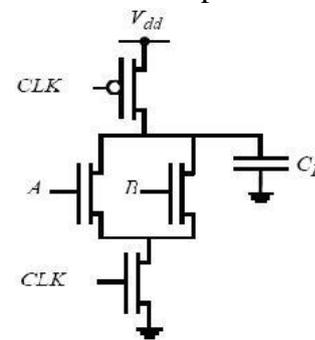


Figure 3(b) Dynamic NOR circuits

We also use pass transistor logic to exploit reduced swing to lower power.

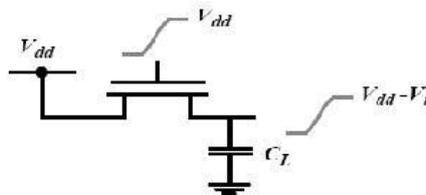


Figure 4. Pass Transistor Logic, $P = CL * Vdd * (Vdd - Vt)$

7.4. REDUCING GLITCHES

Glitches generate in a logic chain when two parallel driving common gate approaches at different times. The output instantly switches to incorrect value before settling to correct value. Consider circuit shown below. Consider that in the absence of buffer path A is high speed and Path B is slow. At beginning if A=0 and B=1 then Z=0. Next if B switched to 0 and A to 1 as B is slow the data 0 arriving at B will be slow and hence Z switches towards 1 for small time before switching back to 0 resulting in unnecessary power dissipation.



Figure 5. Glitch Free AND Gate

7.5. LOGIC LEVEL POWER OPTIMIZATION

During logical design implementation for low power, technology parameters like supply voltage are of fixed value, and availability for selecting the functionality and sizing the gates. Equalizing the path & insertion of buffer is one of the techniques which make sure that signal propagation from inputs to outputs of a logic network follows paths of similar length to overcome glitches. When paths are equalized, there is equal delay for each branch which result in less delay while feeding signal to next node.

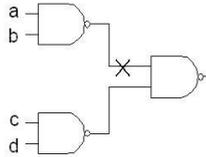


Figure 6. Logic Remapping of design for Low Power^[4]

7.6. STANDBY MODE LEAKAGE SUPPRESSION

Static power & Leakage power generated from substrate currents and sub-threshold leakages. For technologies 1 μm and above, $P_{\text{Switching}}$ was more dominant. But for deep-submicron processes below 180nm, P_{Leakage} becomes dominant parameter. Leakage power is a major issue in recent technologies, as it impacts battery lifecycle & battery life. CMOS technology has been most power-efficient when transistors are not switching or in stand-by mode, and system manufacturer expect low leakage from CMOS IC chips. To meet leakage power parameters, multiple-threshold and variable threshold circuit techniques are frequently used. In multiple-threshold CMOS, the process provides two different threshold transistors. Low-threshold is employed on speed-critical sub-circuits and there are fast and leaky. High-threshold transistors are of low speed but exhibit low sub-threshold leakage, and they are results in noncritical or slow paths of the chip.

7.7. VARIABLE BODY BIASING

Threshold voltage of transistors can be dynamically control by variable-threshold through substrate biasing and hence overcome shortcoming associated with multi-threshold design. When a variable-threshold circuit is on standby mode, the substrate of NMOS transistors is negatively biased, and their threshold increases due to effect of body-biasing. Also the substrate of PMOS transistors is biased by positive body bias to increase their V_t in stand-by mode.^[5] Variable-threshold require control circuits that modulate substrate voltage in stand-by mode. When the circuit is in standby mode the bulk/body of both PMOS and NMOS are biased by third supply voltage to increase the V_t of the MOSFET as shown in the Figure. But in normal operation they are switched back to reduce the V_t .

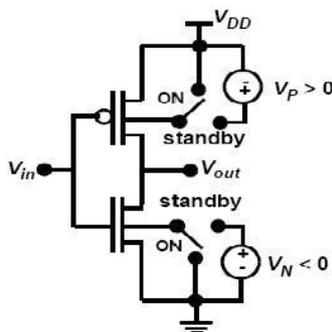


Figure 7. Variable Body Biasing

7.8. SLEEP TRANSISTORS

When High V_t transistors connected in series with low V_t logic as shown below are termed as Sleep Transistor. When Low V_t devices are ON the sleep transistors are also ON resulting in normal operation of the circuit. When the circuit is in Standby mode, High V_t transistors are OFF. As High V_t devices are in series with Low V_t circuit the leakage current is calculated by High V_t devices and is less, thus reduced the power dissipation.

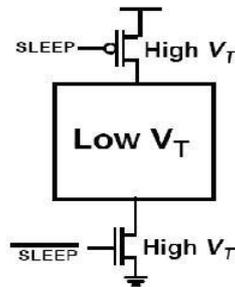


Figure 8. Sleep Transistors Circuit Design

7.9. DYNAMIC THRESHOLD MOS

In dynamic threshold CMOS (DTMOS), the threshold voltage is altered dynamically to suit the operating state of the circuit. For low leakage current we use high threshold voltage in the standby mode & a low threshold voltage gives higher current drives in the active mode of operation. CMOS with dynamic threshold characteristic can be obtained by joining the gate and body with each other. The supply voltage of DTMOS is restricted by the diode built-in potential in bulk silicon technology. The PN diode between source and body must be reverse biased. So, this technique is only preferred for ultralow voltage (0.6V and below) circuits in bulk CMOS.

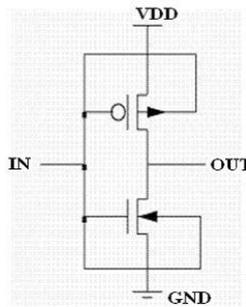


Figure 9. DTMOS Circuit

7.10. SHORT CIRCUIT POWER SUPPRESSION

Short circuit currents that comes into consideration when pairs of PMOS/NMOS transistors are conducting simultaneously resulting in Short circuit power.

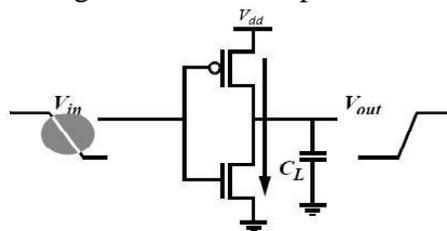


Figure 10. Short Circuit Power in CMOS Circuits

One way to reduce short circuit power is to keep the input and output rise/fall times the same. If the load capacitance is greater, so the output fall time is larger than the input rise time. The drain-source voltage of the PMOS transistor is 0. So the short-circuit power is 0. If the load capacitance is of less capacitance, the output fall time is less than the input rise time. For PMOS transistor the drain-source voltage is nearer to V_{DD} during most of the transition period. Therefore we obtain large short circuit current.

VIII. CONCLUSION

The need for lower power systems is being driven by many market segments. Unfortunately designing for low power adds another dimension to the already complex design problem and the design has to be optimized for power as well as Performance and Area.

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