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A Simulation of Wideband CDMA System on Digital Up/Down Converters

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Abstract— In this paper, I present FPGA implementation of a digital down converter (DDC) and digital up converter (DUC) for a single carrier WCDMA system. The DDC and DUC is complex in nature. The implementation of DDC is simple because it does not require mixers or filters. Xilinx System Generator and Xilinx ISE are used to develop the hardware circuit for the FPGA. Both the circuits are verified on the Spartan - 3 FPGA.

Keywords— WCDMA, FPGA, DDS, FIR

I. INTRODUCTION

Digital down converter (DDC) and Digital up converter(DUC) are extensively used in the radio systems. They are more popular than their analogue counterparts because of small size, low power consumption and accurate performance. The DDC converts the signal at the output of analog to digital converter (ADC), centered at the intermediate frequency (IF), to complex baseband signal. In addition, DDC also decimates the baseband signal without affecting its spectral characteristics. The decimated signal, with a lower data rate, is easier to process on a low speed DSP processor. Similarly, the DUC converts a baseband signal to a passband IF signal. The functional behaviors of the two circuits are therefore equal and opposite. This paper discusses the DDC and DUC for the WCDMA system and implements them on the field programmable gate array (FPGA). WCDMA is a leading choice of data communication in the wireless industry nowadays and is selected as the air interface for the UMTS. WCDMA supports a higher data rate then CDMA and is less susceptible to narrowband interferers and multipath fading. Similarly, FPGAs are used for real time implementation of the signal processing algorithms, particularly related to communication, because of their high speed and accurate performance. I have organized this paper as follows. Section II presents the working principle and FPGA design of the DUC. Section III presents FPGA implementation of the DDC. Section IV presents WCDMA Based System. Experimental results are given in Section V. Finally, this paper is concluded in Section VI.

II. DIGITAL UP CONVERTER

Digital up converter (DUC) converts a baseband low data rate signal to a high data rate intermediate frequency (IF) signal. This is done by first up-sampling the baseband signal to the required sampling frequency and then mixing it with the high frequency carrier. A functional diagram of the DUC is given in Figure l.

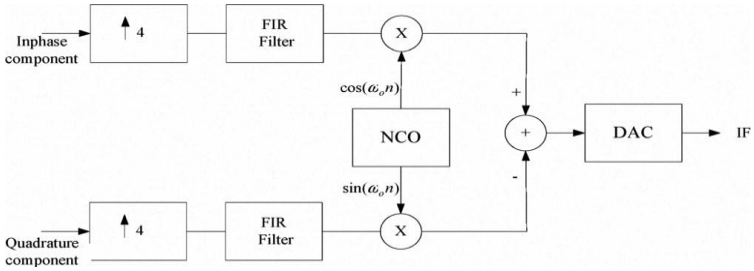

Figure1. Block diagram of digital up converter

The DUC has two identical data paths, one for the inphase and the other for quadrature input. For this reason, it is also referred to as a complex DUC. The baseband signal at 23.04 Msps is upsampled by 4 to 98.16 Msps before mixing with the numerically controlled oscillator (NCO) output, to produce the spectrum centered around the desired modulation frequency. The lowpass FIR filter acts as an anti-alaising filter after upsampling. The specifications of this FIR filter are given in Table 1.

Table1. Specifications for FIR filter in DUC

Stopband frequency	20 GHZ
Passband frequency	5 GHZ
Passband ripple	0.1 dB
Stopband ripple	140 dB

The circuit for the DUC realized on Spartan 3 - FPGA. XILINX ISE Design Tool together with the Xilinx FIR Compiler is used to create a lowpass filter having the above frequency response. The Xilinx DDS Compiler generates the IF carrier frequency signal. Direct digital synthesizer (DDS), a digital version of the NCO, provides an accurate programmable frequency up to 450 GHz.

III. DIGITAL DOWN CONVERTER

The DDC performs the reverse function of the DUC. It converts an IF signal to the baseband signal. The DDC is built in a similar manner as DUC, but it uses down-sampling instead of up-sampling and they are connected in the reverse order compared to the DUC. This paper uses the DDC as described in [1] for the FPGA implementation. A functional block diagram of the DDC is shown in Figure 2. This DDC does not require mixers or low pass filters [1].

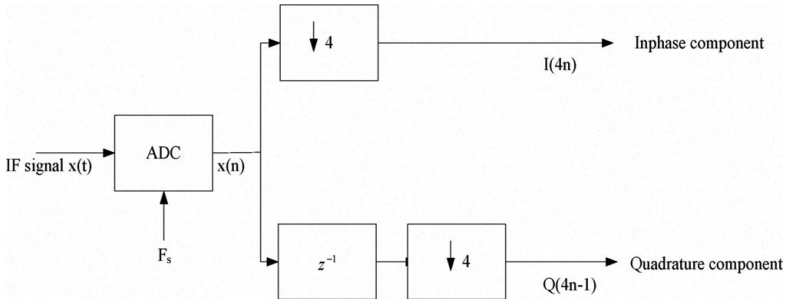

Figure2. Block diagram of digital down converter

The IF signal *x(t)* is sampled at 98.16 Msps by the ADC to create a digitized IF signal *x(n)* . This signal is demultiplexed into two data streams. One signal stream is downsampled by 4 to produce an inphase signal *I(4n)*,while the other stream, delayed by a single sample, gives the quadrature

component Q(*4n* -1) on downsampling . The data rate of resultant inphase and quadrature signals is 23.04Msps. Mathematical analysis of DDC is given in the Appendix.

IV. WCDMA BASED SYSTEM

WCDMA (Wideband Code Division Multiple Access) is the radio access scheme used for third generation cellular systems that are being rolled out in various parts of the globe. The 3G systems to support wideband services like high-speed Internet access, video and high quality image transmission with the same quality as the fixed networks. In WCDMA systems the CDMA air interface is combined with GSM based networks. The WCDMA standard was evolved through the Third Generation Partnership Project (3GPP) which aims to ensure interoperability between different 3G networks. The standard that has emerged through this partnership project is based on ETSI's Universal Mobile Telecommunication System (UMTS) and is commonly known as UMTS Terrestrial Radio Access (UTRA). The access scheme for UTRA is Direct Sequence Code Division Multiple Access (DS-CDMA). The information is spread over a band of approximately 5 MHz this wide bandwidth has given rise to the name Wideband CDMA or WCDMA.

V. EXPERIMENTAL RESULTS

The DDC and DUC circuits created using the Xilinx System Generator are finally converted to bit file using the Xilinx ISE. The FPGA used is Spartan-3. WCDMA signal at IF 23.04 MHz is generated using the signal generator and applied to the ADC. Focusing on the physical layer, notice that a radio chip and a base-band chip are typically used with analog transmit and receive interfaces. The base band chip is mostly a digital circuit, containing only data converters as analog blocks. This system partitioning minimizes the digital switching noise coupling into the radio sections and provides low power chip-to-chip analog interfaces. The radio chip may be designed in different technologies such as Si bipolar, SiGe, BiCMOS, or recently, even in straight CMOS. Typically, a -75dBm sensitivity is accomplished for about 200 mW receiver power dissipation. The radio architecture has evolved from a conservative super heterodyne approach to less expensive direct down/up conversion. The efficiency of the linear power amplifier is limited by the signal peak-to-average ratio, which is moderate, allowing reasonable transmitter power dissipation, typically 500 mW.

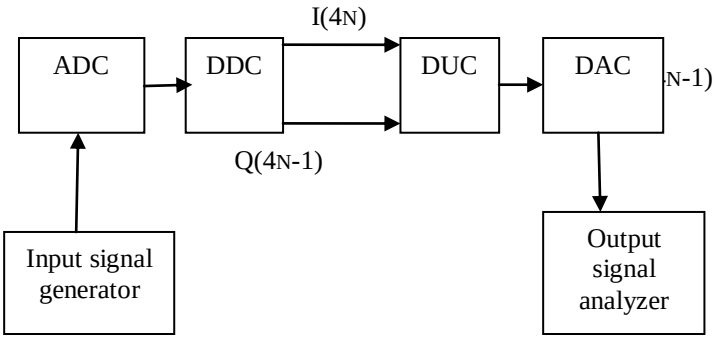

Figure3. Xilinx ISE Laboratory test bench

Table2. Parameters used in test bench

Parameter	Value
FPGA	Xilinx Spartan-3A [(XC3S700A [N]-FG484)
FPGA clock frequency	126.441 MHZ
Sampling frequency	126.441 MHZ
Input data rate	3.84 Msps
IF frequency	23.04 MHZ

Figure 4 shows the simulation of the baseband signal at the output of DDC. The bandwidth of this signal is 5 MHz.

Similarly, It shows the simulation of the IF signal at the output of DUC. A brief summary of FPGA resource utilization as given by Device Utilization Summary in Xilinx ISE is given in Table 3.

Table3. FPGA resource utilization

Logic Utilization	Used	Available	Utilization
Number of Slices	802	3584	22%
Number of Slice Flip Flops	1142	7168	15%
Number of 4 input LUTs	833	7168	11%
Logic Utilization	Used	Available	Utilization
Number of bonded IOBs	47	141	33%
Number of GCLKs	1	8	12%

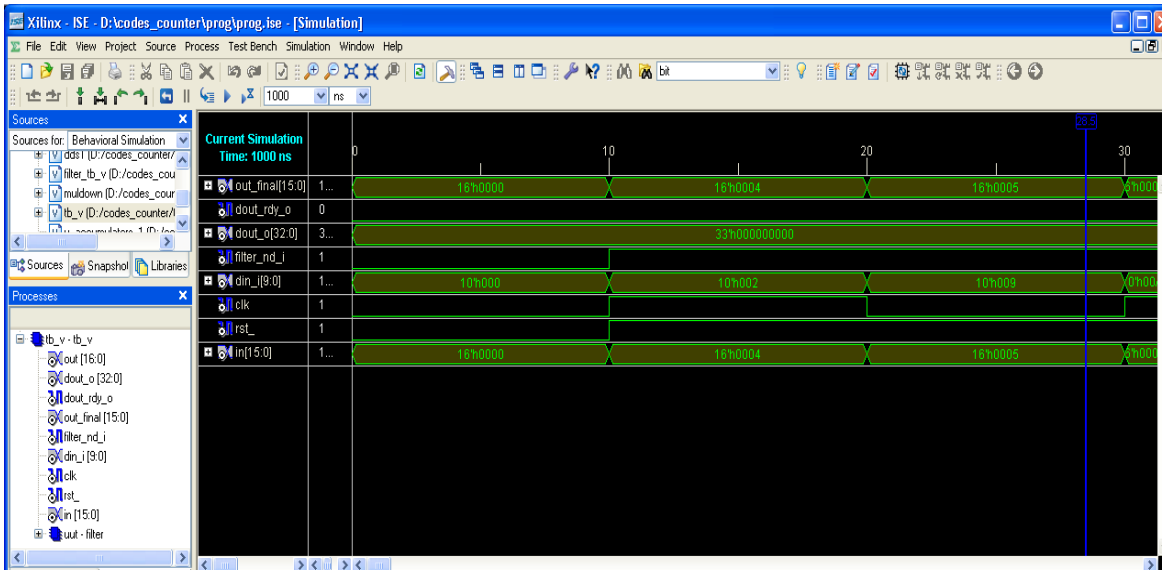

Figure4. Simulation of Digital up/down converter on WCDMA signal

Inputs: din (dac input), in(main), clk(clock), filter_nd_i(filter I/P), rst_(Reset)
Outputs: dout_o(dac output), out (filter O/P), out_final(final output), dout_rdy_o(enables for o/p)

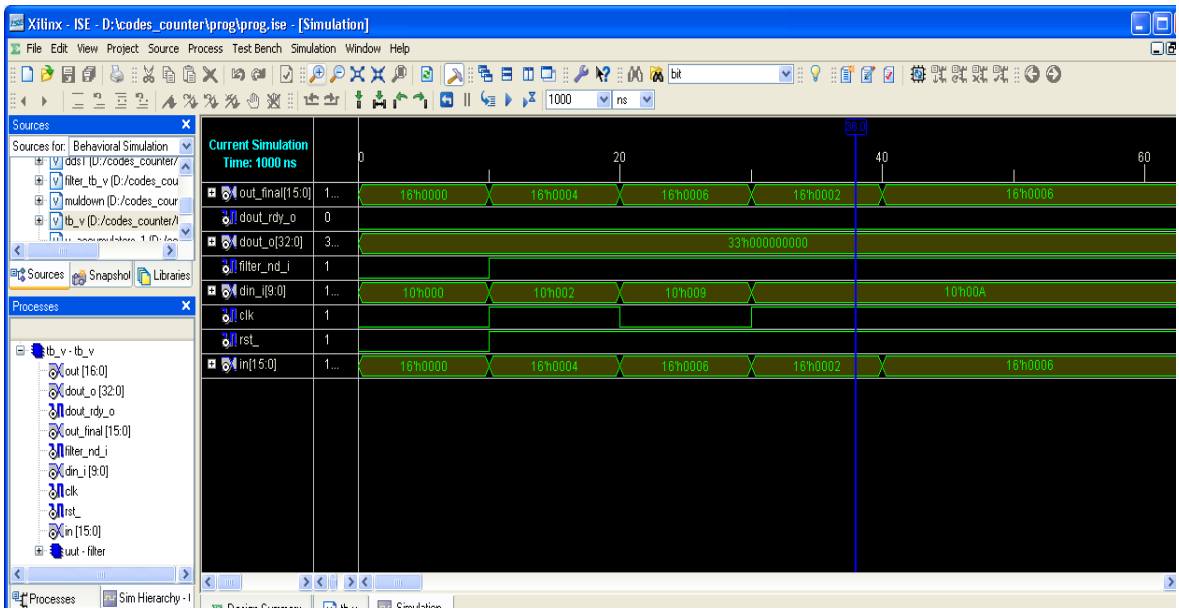

Figure4. Simulation of Digital up/down converter on WCDMA signal

VI. CONCLUSION

A Digital up/down converter was designed and implemented on Spartan-3 FPGA kit. The codes were written using Verilog and simulated. The Work Involves High Speed, High Bandwidth, High transfer rate, less timing from digital down to up frequency conversion for wide-band code division multiple access spectrums used in 3G mobile telecommunications network systems. It utilizes DS-CDMA channel access method and FDD duplexing method to achieve higher speeds and support more users compared to most time division multiple access schemes used today. WCDMA transmits on a pair of 5MHz-wide radio channels.

APPENDIX

$$x(n)= I(n)Co\{\pi/2\ n)-Q(n)sin(\pi/2\ n) \qquad \textbf{--(1)}$$

$$x(n-1) = \mathrm{I(n-1)Cos}(\pi/2\ (n-1))-Q(n-1)\ \sin\ (\pi/2\ (n-1))$$
$$= \mathrm{I(n-l)sin}(\pi/2\ n)+Q(n-1)cos\{\ \pi/2\ \ n) \qquad \textbf{--(2)}$$

Inphase component

$$x(n-\ 2) = I(n-2)\ \sin\ (\pi/2\ (n-1))-Q(n-2)Cos(\pi/2\ (n-1))$$
$$=-I(n-2)Cos\{\ \pi/2\ n)+Q(n-2)Sin(\pi/2\ n)$$

Downsampling by a factor of 4,

$$X(4n-2)= -I(4n-2)Cos\{\ 4\ (\pi/2)n)+0$$
$$= -I(4n-2)$$

Passing through the filter, we get the inphase component

$$x(4n-2) = I(4n-2)$$

Quadrature component

From Equation (2),

$$x(n-\ 2) = I(n-2)\ \sin\ (\pi/2\ (n-1))-Q(n-2)Cos(\pi/2\ (n-1))$$
$$= -I(n-2)Cos\{\ \pi/2\ n)+Q(n-2)Sin(\pi/2\ \ n) \qquad \textbf{--(3)}$$

Delaying Equation 3 by one sample,

$$x(n-3) =-I(n-3)Sin(\pi/2\ n)-Q(n-3)Cos\{\ \pi/2\ \ n)$$

Downsampling by a factor of 4,

$x(4n- 3)=-Q(4n-3)$

Passing through an filter,

$x(4n-3)= Q(4n-3)$

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