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LOW VOLTAGE LOW DROPOUT REGULATOR USING CURRENT SPLITTING TECHNIQUE

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Abstract - We proposed a low voltage low dropout regulator that converts an input of 1 v to an output of 0.85-0.5 v with 90-nm CMOS technology. Current splitting technique used to boost the gain by using an error amplifier. A power noise cancellation mechanism is formed in the rail-to-rail output stage of the error amplifier, to minimize the size of power MOS transistor. In this paper we achieve a fast transient response, high power supply rejection, low dropout regulator, low voltage, and small area. CMOS processes have been used in Large scale integrated circuits like LSI and microprocessor they have been miniaturized constantly. Taking full advantage of the miniaturization technology, CMOS linear regulators have become the power management ICs that are widely used in portable electronics products to realize low profile, low dropout, and low supply current.

Keywords- LDO regulator, CMOS technology, small area, Fast transicent reponse, High stability,

I. INTRODUCTION

Low-dropout regulators (LDO) are widely used in electronics products due to their precision output voltage and less prone to noise. The advancement in battery operated portable devices, noise sensitive devices and other devices, which need high precision supply voltages has fuelled the growth of Low Drop-Out Regulators. Low Drop-Out
Regulators have shown advantage over its counterpart. The design of Low Drop-Out Regulators with high performance is challenging problem now-a-days. An important building block in power management is the low drop out linear regulator which often follows a dc-dc switching capacitor.

A Low Drop-out regulator is a circuit that provides a well-specified and stable DC voltage whose input to output voltage difference is low. The dropout voltage is defined as the value of the input/output differential voltage where the control loop starts regulating.

II. RELATED WORKS

Bandwidth is an important specification in voltage regulator design. The higher the bandwidth of a regulator, the more quickly it can react to changes in input and power supply and keep the output voltage constant. High bandwidth also improves the power supply rejection ratio (PSRR) of the regulator, which is a measure of how well the regulator attenuates noise on the power supply. The better power supply rejection, the less the output voltage changes in response to fluctuations in the supply. Therefore, to achieve good specifications, a novel LDO with a very simple circuit structure is employed. Low –power Low-voltage microprocessors implemented in a scaled CMOS technology often require multiple supply voltages. CMOS circuit operating at a constant frequency reduces the supply voltage.

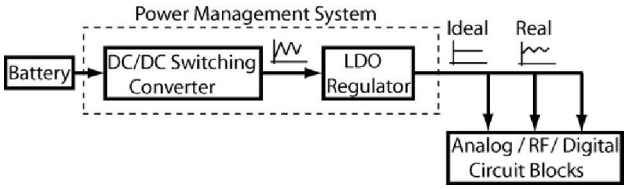

Figure 1. Power management

A. Feed Forward Ripple Cancellation Technique-

The Feed forward Ripple Cancellation LDO achieves a high power supply rejection over a wide frequency range. Kelvin connection is also used to increase the gain bandwidth of the LDO allowing for faster transient performance. The LDO is implemented in 0.13 m CMOS technology and achieves a power supply rejection better than 56 dB up to 10 MHz for load currents up to 25 m A. Load regulation of 1.2 mV for a 25 m A step is measured, and the whole LDO consumes a quiescent current of 50 A with a band gap reference.

B. Buffer Impedance Attenuation Technique

A low-dropout regulator for an impedance - attenuated buffer for driving the pass device. Dynamically - biased shunt feedback is proposed in the buffer to lower its output resistance such that the pole at the gate of the pass device is pushed to high frequencies without dissipating large quiescent current. By employing the current buffer compensation, only a single pole is realized within the regulation loop unity gain bandwidth and over 65 phase margin is achieved under the full range of the load current in the LDO. The LDO thus achieves stability without using any low-frequency zero. The maximum output-voltage variation can be minimized during load transients even if a small output capacitor is used. The LDO with the proposed impedance-attenuated buffer has been implemented in a 0.35 um twin-well CMOS process. The proposed LDO dissipates 20- A quiescent current at no-load condition and is able to deliver up to 200-mA load current. With a 1- F output capacitor, the maximum transient output-voltage variation is within 3% of the output voltage with load step changes of 200 m A / 100 ns.

C. Ultra-Fast Load Regulation Technique

In this method we demonstrate a fully integrated linear regulator for multi supply voltage micro processors implemented in a 90 nm CMOS technology. Ultra-fast single-stage load regulation achieves a 0.54-ns response time at 94% current efficiency. For a 1.2-V input voltage and 0.9-V output voltage the regulator enables a 90 mV P-P output droop for a 100-mA load step with only a small on-chip decoupling capacitor of 0.6 n F. By using a PMOS pull-up transistor in the output stage we achieved a small regulator area of 0.008 mm2 and a minimum dropout voltage of 0.2 V for 100 m A of output current. The area for the 0.6-n F MOS capacitor is 0.090 mm^2.

III. PROPOSED SYSTEM

In this paper we use the power management scheme as the switching regulators and post regulators.

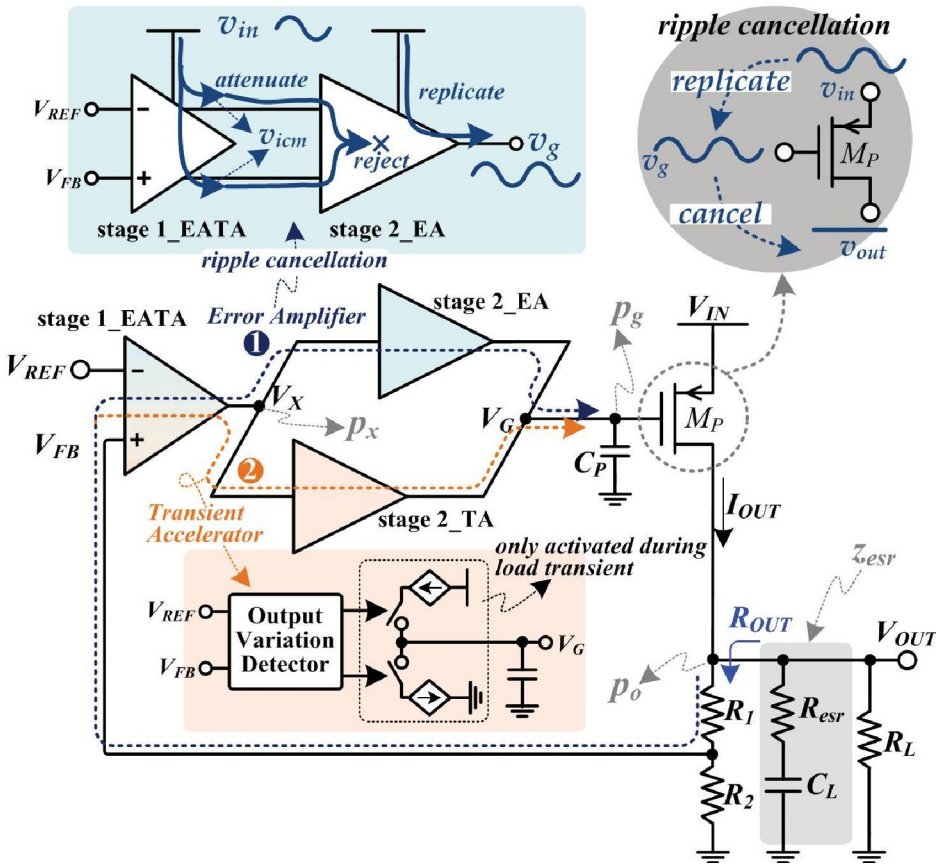

Figure2.Block Diagram of Proposed LDO regulator

Primary switching regulators converts the high dc voltage level of the battery into low dc voltage level of the battery with high conversion energy. It generates voltage ripples over the range of switching frequency.

A. Low Supply (Input) Voltage and Low IQ

A high loop gain is mandatory in LDO regulator design to achieve optimum performance values such as accurate output (line/load regulation) and PSR. A low supply voltage and output-resistance reduction induced by a shrinking technology limit the achievable gain of the EA. Thus, there are many auxiliary circuits that consume considerable *IQ* that are proposed to enhance performance.

B. Fast Transient Response

The transient response, includes the voltage variation (spike) and recovery (settling) time during the load current transient. The voltage variation is more important than the recovery time, as even a small output-voltage variation (e.g., 50 mV) can cause severe performance degradation to the load circuit operating at an ultralow supply voltage (e.g., 0.5 V). To reduce the output-voltage variation, both a large closed-loop bandwidth of the LDO regulator and a large output current slew rate of the EA are required.

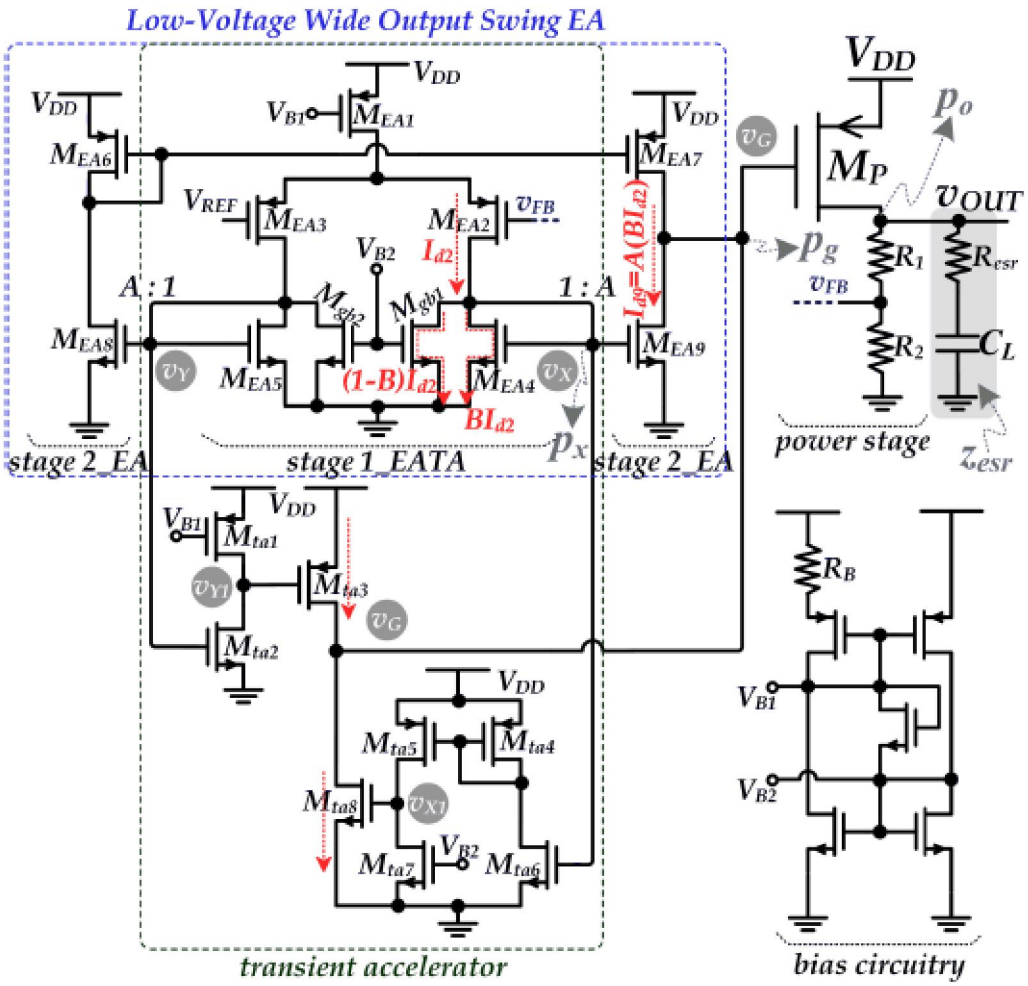

Figure3.Circuit schematic of the proposed LDO regulator

C. Power Supply Rejection

To provide a clean and accurate output voltage with a low voltage level (≤1 V), noise suppression is paramount. An *n*-type power MOS transistor or a cascoded power MOS transistor structure can achieve a high PSR; however, they are unfeasible for sub 1-V operations. As an LDO regulator adopts a *p*-type power MOS transistor, either a high loop gain or good noise cancellation at node *V*G can achieve a high PSR.

D. Small Area

In a low-voltage LDO regulator design, several performance enhancing auxiliary circuits and a large *MP* occupy considerable space. A wide output swing EA can reduce the size of the *MP*. To support a wide load current range (e.g., 0–100 mA) and a wide output-voltage range (e.g., 0.5–0.85 V), the *MP* may enter the triode region when under a heavy load condition (large *V*SG*)* with a low-dropout voltage (small *V*SD*)*. The *MP* should, therefore, be large enough to make the intrinsic gain of the *MP* close to one at the triode region and maintain a high loop gain in the LDO regulator.

E. Stability

The dominant pole for an off-chip capacitor (e.g., *CL* = 1 μF) compensated LDO regulator, exists at the output node. As a large *MP* contributes the first nondominant pole (*pg)* at a relative low frequency, a large equivalent series resistance of *CL* (*R*esr*)* is required to generate a low frequency zero (*z*esr*)* to cancel *p*g. Therefore, large output variations during the load transient are induced by the large *R*esr. A wide output swing EA can reduce the size of the *MP* implying that such pole-zero cancellation is taking place at a higher frequency with a related small *R*esr .

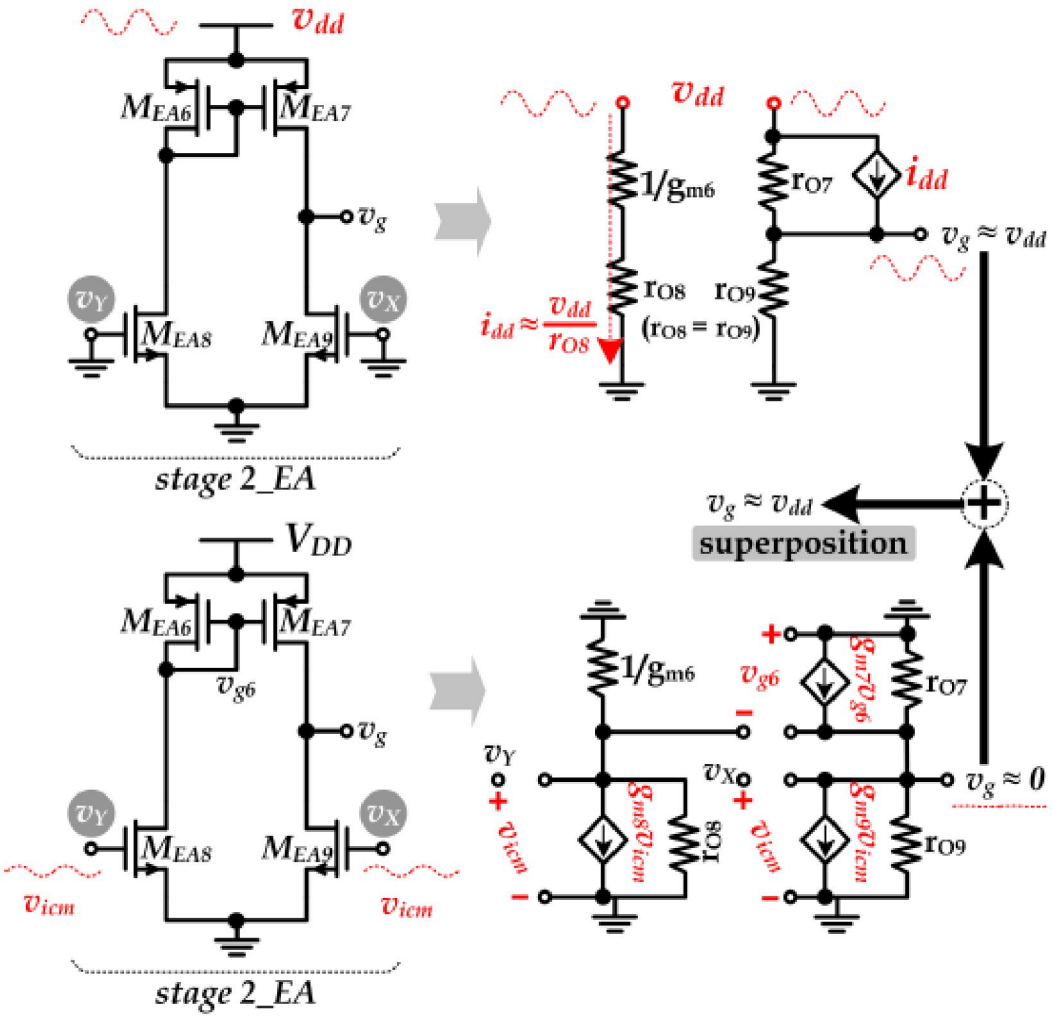

Figure4.Low-frequency, small-signal model of the EA output stage (stage 2_EA) for ripple cancellation analysis

IV. CONCLUSION

This paper achieved the fast transient response, low Iq and high PSR under wide range of operating conditions. Proposed LDO regulator was designed using a 90 nm CMOS process to convert an input of 1v to an output of 0.85-0.5 v, while achieving a PSR of ~50 dB with a 0-100 kHZ frequency range. A 28 mV maximum output variation for a 0-100mA load transient, and a 99.94% current efficiency achieved.

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