

## **FPGA IMPLEMENTATION OF UNIVERSAL SHIFT REGISTER FOR ASYNCHRONOUS DATA SAMPLING**

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**Abstract**—Now a days power consumption plays a vital role in vlsi circuits. The growing market of mobiles, battery-powered electronic devices demands the design of electronic circuits with low power consumption. To design a low power circuit, energy efficiency from the clock element is an important issue. There are different technique for the energy efficiency. One technique for efficiency is the use of double edge-triggered flip-flops (DETFs), since they can maintain the same throughput as single edge-triggered flip-flops (SETFFs) while only using half of the clock frequency. Double-edge triggered (DET) flip-flops are bistable flip-flop circuits in which data is latched at either edge of the clock signal. Using such flip-flops permits the rate of data processing to be preserved while using lower clock. Therefore, power consumption in DETFF based circuit may be reduced. The DETFF designs provide the best performance not only in power but also in speed. Clock gating is another well-accepted technique to reduce the dynamic power of idle modules or idle cycles, like the power wasted by timing components during the time when the system is idle. Clock gating means disabling the clock signal when the input data does not alter the stored data. However, incorporating clock gating with DETFFs to further reduce dynamic power consumption introduces an asynchronous data sampling (i.e., a change in output between clock edges). In this paper are discussing two different methods to avoid asynchronous data sampling and implement this using universal shift register.

**Keywords**- DETFFs, clock-gating, asynchronous data sampling, SETFFs, DHSCGFF, A/MS.

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### **I. INTRODUCTION**

In the past, the major concerns of VLSI designer were area, Performance, cost and reliability. power consideration were mostly of only secondary importance. In recent years, however, this has begun to change and increasingly power has being given comparable weight to area and speed in VLSI design. The widespread use of mobile devices in modern society, power efficiency and energy savings become extremely important issues for designers. Normally, high performance chips have high Integration density and high clock frequency, which tend to dictate power consumption. Therefore, designs are needed that can consume less power while maintaining comparable performance. Power consumption in the conventional CMOS digital circuit can be separated into three types of power dissipation: (i) switch power, (ii) short-circuit power, and (iii) leakage power consumption. The switching power represents the power dissipated during the signal transitions when energy is drawn from the power supply to charge-up the device capacitances. Short-circuit power is produced during the moment that both the PMOS network and the NMOS network are simultaneously on in CMOS logic. The MOSFETs in CMOS logic normally will have some non-zero reverse leakage and sub-threshold current, which causes the leakage power consumption. The sum of switching power and short-circuit power can be categorized as dynamic power, while the leakage power also called static power dissipation. The static power increases faster than dynamic power with the shrinking of feature size.

As a commonly used component in the digital system, flip-flops often appear in computational circuits or are used as registers in pipeline structures to store the data for additional processing. The conventional single edge-triggered flip-flop is usually implemented by cascading two oppositely phased latches, and is active on either the rising edge or the falling edge of the clock. During the first half of the clock cycle, the primary latch loads the input. Then the data value is passed to the secondary latch during the next half of the clock cycle. To take advantage of that idle edge, double edge-triggered flip-flops have emerged. The DETFF requires a lower clock frequency than the SETFF to achieve comparable performance. As timing components, flip-flops capture data with the active edge of the clock signal, sometimes this capture is not necessary because the data value is unchanged. Because of the constant activity of the clock signal, timing components that respond on the clock transition are the most power-consuming components in the VLSI system. The most obvious power reduction is to prevent transitions made by the clock while the input data value matches the current state. So clock-gating techniques have been developed to disable unnecessary clock switching when there is no change on the input to the flip-flop.

## **II. SCOPE OF THE WORK**

Power-reducing techniques have been added to DETFFs in order to save the power dissipated on the clock tree. Clock-gating is one of the major techniques. For a large digital system, clock-gating technique is used to reduce the power consumed on idle circuitry in the design. It can be applied at both behavior-level and circuit level. To further reduce the power consumption clock-gating technique used with DETFFs. However, the combination of clock-gating and double edge-triggered techniques can create an asynchronous sampling under certain circumstances.

A specialized gating circuit for DETFFs is proposed and this circuit is evaluated for their effectiveness to address the asynchronous data sampling. An approach is designed to filter out the asynchronous data sampling by only resuming the connection between the global clock and the internal clock when they are in phase. This paper discusses the analysis of recent attempts to include clock-gating technique with synchronous double edge-triggered mechanisms. For a clock-gated system, the internal clock controls the gated circuits. During the gated periods, the internal clock is separated from the global clock. If the internal clock is out of phase with the global clock when the gating signal is de-asserted, then the internal clock signal switches immediately to match the global clock. This internal clock switch is extra and not synchronized with the external clock, which creates an asynchronous data sampling, evidenced by the output changing between clock edges. Each clock gating transition has the potential to create the asynchronous sampling issue. Since the issue is not always present, the analysis examines the specific conditions that create the asynchronous data sampling.

## **III. RELATED WORKS**

### **3.1. Low-power clock branch sharing double edge triggered flip-flop**

The clock system, which consists of the clock distribution network and timing elements (flip-flops and latches), is one of the most power consuming components in a VLSI system. It accounts for 30% to 60% of the total power dissipation in a system. As a result, reducing the power consumed by flip-flops will have a deep impact on the total power consumed. Voltage scaling is the most effective way to decrease power consumption, since power is proportional to the square of the voltage. However, voltage scaling is associated with threshold voltage scaling which can cause the leakage to increase exponentially. Besides supply voltage scaling, double-edge clocking can be used

to save half of the power on the clock distribution network. Cutting the frequency of the clock by one half will halve the power consumption on the clock distribution network.

The reduction of energy consumption has become one of the most important factors in digital systems design, due to the increasing use of portable computing and communication systems. The clock system, composed by flip-flops and a clock distribution network, is one of the most power-consuming subsystem in a VLSI circuit. As a consequence, many techniques have been recently proposed to reduce clock system power dissipation, including reduced voltage-swing clocking schemes, the use of gated clocks, and the introduction of flip-flop circuits with a reduced number of clocked transistors. The DETFF design will use more clocked transistors than SETFF design generally. However, the DETFF design should not increase the clock load too much. The DETFF design aim at saving energy both on the distribution network (by halving the frequency) and flip-flops. It is preferable to reduce circuits clock loads by minimizing the number of clocked transistors. Furthermore, circuits with reduced switching activity would be preferable. Low swing capability is very helpful to further reduce the voltage on the clock distribution network for power saving, if applicable. Due to the fact that voltage scaling can reduce power efficiently, the cluster voltage scaling systems are widely used.

### **3.2. Low- power double edge triggered flip-flop circuit design**

This compare three previously published static double edge-triggered (DET) flip-flops with a proposed design for their transistor counts and power consumptions. The proposed DET flip-flop uses only 12 transistors in addition to the clock driver, and hence requires a small area. In a conventional single edge-triggered (SET) flip-flop, data move from input to output in synchrony with one edge of the clock. The use of double edge-triggered (DET) flip-flops has been proposed for low-power circuit design. In a DET flip-flop, both rising and falling edges of the clock signal are used to transfer data from input to output. In this way, for a given throughput, the clock frequency can be halved with respect to a system using SET flip-flops, with a reduction of power dissipation. Unfortunately, DET flip-flops require a more complex implementation with respect to SET structures. This results not only in larger silicon area but also in a higher number of internal nodes and switching capacitance, which may offset the advantages of a reduced clock frequency. Furthermore, that power dissipation of DET flip-flops is more sensible to input signal glitches with respect to standard single edge-triggered flip-flops.

Conventional DETFF duplicate the latching component, hence duplicating the area and increasing the input loads. The explicit double edge pulsed flip-flops have an external pulse generator, so they have higher power consumption. The clock branch sharing implicit pulsed flip-flop uses a clock branch sharing scheme to sample the clock transitions, which efficiently reduces the number of clocked transistors and results in lower power while maintaining a competitive speed. It employs the conditional discharge technique and the split path technique to reduce the redundant switching activity and short circuit current, respectively. This flip flop has the least 5 number of clocked transistors and lowest power. Hence, it is suitable for use in high-performance and low-power environments.

### **3.3. Double edge triggered half-static clock gated D-type flip-flop**

This paper proposes a double edge-triggered half-static clock-gated D-type flip-flop (DHSCGFF), which consists of two parallel dynamic master latches connected in parallel and a single half-static latch with clock-gating circuit. The proposed DHSCGFF makes use of a clock-gating circuit to achieve better race tolerance, circuit compactness and energy efficiency without the use of pulse generator. Simulation results of the proposed circuit using a 0.18  $\mu\text{m}$  technology is

presented. Results indicate that the proposed circuit can achieve a 4 Gbits/sec data rate and a 96% redundant power reduction.

In order to save on clocking power, dual-edge triggered (DET) clocking strategy uses DET storage elements that capture the value of the input after both rising and falling clock transitions. Otherwise, DETSE is nontransparent, i.e., it holds the captured value at the output. Thus, the DET clocking strategy provides a one-time solution to the frequency scaling by retaining the data throughput of single-edge triggered (SET) clocking at halved clock frequency. However, in order to fully exploit the power savings in the clock distribution network, this approach must ensure that the delay and energy consumption of DETSE must be comparable to those of SET storage elements. Furthermore, use of both clock edges to synchronize the operation makes timing sensitive to clock duty cycle and increases clock uncertainties generated by the clock distribution system.

### **3.4. A low power double edge triggered flip-flop with transmission gates and clock gating**

In recent years, energy saving techniques have become critical in hardware designs, especially for mobile devices. This paper has reviewed several previous designs of double edge-triggered flip-flops, and has proposed a transmission-gate-based double edge-triggered flip-flop with a clock-gating function. Comparing to the previous work of double edge-triggered flip-flops, the proposed one saved 33.14% power on average and it can save up to 97.85% power compared to conventional single edge-triggered flip-flops when the input is idle. The sequential circuits in a system are considered major contributors to the power dissipation since one input of sequential circuits is the clock, which is the only signal that switches all the time. In addition, the clock signal tends to be highly loaded. To distribute the clock and control the clock skew, one needs to construct a clock network (often a clock tree) with clock buffers. All of this adds to the capacitance of the clock net. The clock signals in digital computers consume a large (15–45%) percentage of the system power. Thus, the circuit power can be greatly reduced by reducing the clock power dissipation. Most efforts for clock power reduction have focused on issues such as reduced voltage swings, buffer insertion, and clock routing. In many cases, switching of the clock causes a great deal of unnecessary gate activity. For that reason, circuits are being developed with controllable clocks. This means that from the master clock other clocks are derived which, based on certain conditions, can be slowed down or stopped completely with respect to the master clock.

A technique for saving power in the clock tree is by stopping the clock fed into idle modules. However, there is a number of issues related to the design of the clock tree. A technique is used to generate a signal to control the load enable pin of the flip flops in the data path. The control signal is derived by investigating the relationship between the latched input and the primary outputs of the combinational blocks in the data path. The technique is useful only if the outputs of the block can be pre-computed (predicted) for certain input assignments. Another technique use a latch to gate the clock in control dominated circuits. The problem is that the additional latch receives the clock's triggering signal, which results in extra power dissipation in the latch itself. Besides, this scheme results in the derived clock having a considerable skew with respect to the master clock.

## **IV. MATERIALS AND METHODOLOGY**

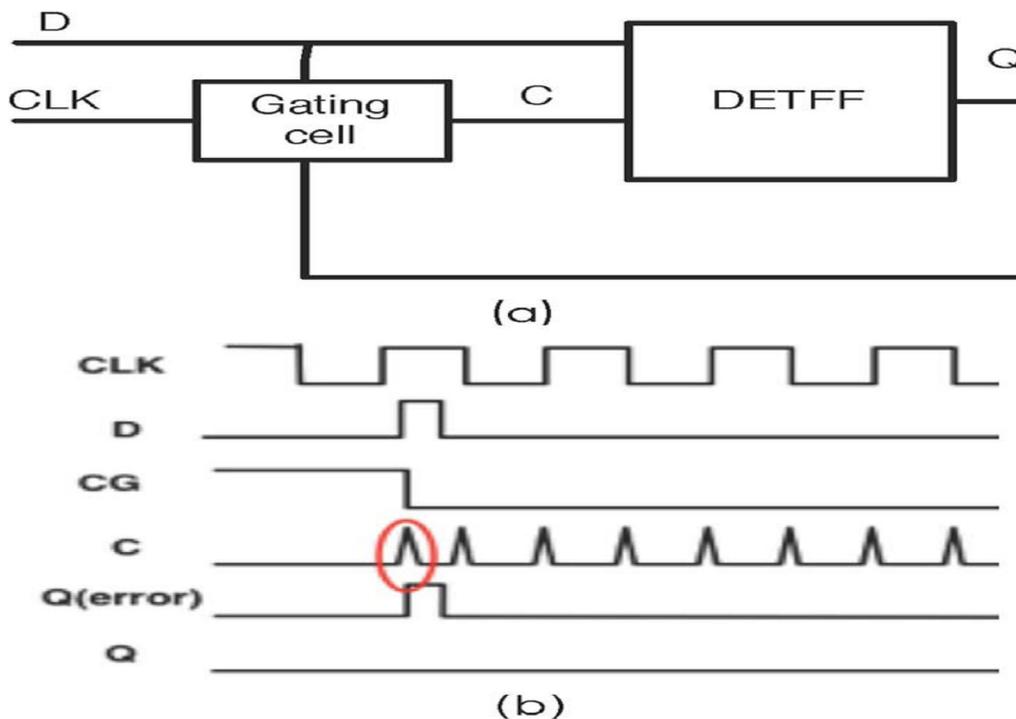
### **4.1. Tanner**

Tanner EDA provides of a complete line of software solutions for the design, layout and verification of analog and mixed-signal (A/MS) ICs and MEMS. Customers are creating breakthrough applications in areas such as power management, displays and imaging, automotive, consumer electronics, life sciences, and RF devices. A low learning curve, high interoperability, and a powerful user interface improve design team productivity and enable a low total cost of ownership (TCO).

Capability and performance are matched by low support requirements and high support capability as well as an ecosystem of partners that bring advanced capabilities to A/MS designs. Tanner Tools v16 offers many new features and significantly greater functionality. Tanner EDA software tools for A/MS and MEMS design offer designers a seamless, efficient path from design capture through verification. The Tanner EDA full-flow design suite offers designers solutions for analog, mixed-signal, RF and MEMS IC design with a seamless, efficient path from design capture through verification. Integrated tool suite with solutions for schematic capture, circuit simulation, and waveform probing to physical layout and verification. HiPer Silicon shares a common architecture and common User Interface that is consistent across all tools, resulting in a comprehensive, unified software solution that maximizes design productivity while simultaneously reducing total cost of ownership. HiPer Silicon's advanced features and optional add-in tools improve designer productivity, including Verilog-A simulation, device layout automation, interactive auto routing, foundry-compatible physical verification and parasitic extraction. HiPerDevGen accelerates rather than automates the environment; maintaining the artistic nature of the process while allowing engineers to meet market demands for quality and cycle time. Physical layout – L-Edit Pro includes layout editing, Interactive DRC for real-time design rule checking during editing, Standard DRC for hierarchical DRC, Standard Extract for netlist extraction, Standard LVS for layout versus schematic, Node Highlighting for highlighting all geometry associated with a node and SPR for standard cell place & route.

#### **4.2. Analysis of asynchronous data sampling**

For double edge-triggered D-type flip-flops, there are eight possibilities when considering factors of: (1) the next input, (2) the present output, and (3) the active clock edge. Four scenarios hold the previous value, and the other four enable a data transition. There are four cases that enable a data transition in a D flip-flop: Before rising edge: (1) Q=0, D=1, (2) Q=1, D=0. Before falling edge: (3) Q=0, D=1, (4) Q=1, D=0. There will be 50% possibility to have an asynchronous data transition when clock gating is turned off. There are different implementations of a DETFF with clock gating which shows how the asynchronous data sampling occurs. The asynchronous data sampling causes the discontinuity between the global and internal clock. When clock gating is discontinued and if the internal clock differs from the global clock, the internal clock event is transmitted immediately. CLK is the global clock; CG is the signal to enable or disable clock gating; C is the internal clock pulse; D is the input; Q (error) is the output under the impact of asynchronous data sampling; Q is the correct output.



**Figure 1. (a) Generic block diagram of clock gated DETFF  
 (b) Example of data miscommunication error**

### 4.3. Methods to avoid asynchronous data sampling

**Method A:** When the gating signal is deasserted, only resume the connection of CLK to during  $CLK=C$ , which avoids the asynchronous transition in C.

**Method B:** Always force the clock-gating signal to synchronize with the CLK.

## V. CONCLUSION

The asynchronous data sampling is a general and universal potential error condition associated with the clock-gated DETFF, although some asynchronous transitions may be masked because of circuit capacitances. In this paper, several solutions have been provided to avoid the asynchronous data sampling problem in clock-gated DETFF. Thus the removal of asynchronous data sampling can be achieved in universal shift registers by using above mentioned methods.

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