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FPGA IMPLEMENTATION OF RECOVERY BOOSTING TECHNIQUE TO ENHANCE NBTI RECOVERY IN SRAM ARRAY

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Abstract— Negative Bias Temperature Instability is an important lifetime reliability problem in microprocessors. SRAM-based structures within the processor are especially susceptible to NBTI since one of the PMOS devices in the memory cell always has an input of '0'. Previously proposed recovery techniques for SRAM cells aim to balance the degradation of the two PMOS devices by attempting to keep their inputs at a logic '0' exactly 50% of the time. However, one of the devices is always in the negative bias condition at any given time. In this paper, we propose a technique called Recovery Boosting that allows both PMOS devices in the memory cell to be put into the recovery mode by slightly modifying the design of conventional SRAM cells to verify its functionality and quantity area and power consumption.

Keywords- SRAM, PMOS , Negative Bias Temperature Instability.

I. INTRODUCTION

Negative Bias Temperature Instability is the generation of interface traps under negative bias conditions at elevated temperature in PMOS transistor which manifests as an increase in the threshold voltage and consequent decrease in drain current and trans-conductance of a MOSFET. It has emerged as a major reliability challenge for the semiconductor industry in recent years. NBTI impact is getting worse in each technology generation with greater performance and reliability loss. When a negative voltage is applied at a p-channel transistor (PMOS) gate, interface traps are formed near oxide layer, causing a change in transistor characteristics. When the input to a PMOS is low (logic zero), the transistor is in a stress phase. During the stress phase, the transistor parameters slowly deviate from the nominal value. When the input to the PMOS is high (logic one), the transistor is in a recovery phase. During the recovery phase, trapped charges are released, regaining the original transistor state. The PMOS enters into stress and recovery phases alternately, when the input to the PMOS is dynamic. Longer the stress period, higher is the impact of NBTI on transistor parameters. Therefore, input to the transistor indirectly determines the extent of NBTI degradation.

II. RELATED WORKS

2.1 BASICS OF RECOVERY BOOSTING

The basic idea behind recovery boosting is to raise the node voltages of a memory cell in order to put both PMOS devices into recovery mode in SRAM cells since it has cross coupled inverters. The main contributions of this paper are 1) It describes how SRAM cells can be modified to support recovery boosting and discuss the two basic types of recovery boosting; 2) The circuit for fine-grain and coarse grain recovery boosting is discussed. 3) The simulation results of modified SRAM that supports recovery boosting; fine-grain and coarse grain recovery boosting is compared and analyzed.

2.2 FAILURE ANALYSIS OF ASYMMETRIC AGING UNDER NBTI

Large instruction window processors achieve high performance by exposing large amounts of instruction level parallelism. However, accessing large hardware structures typically required to buffer and process such instruction window sizes significantly degrade the cycle time. A recent work in this area proposes a novel Checkpoint Processing and Recovery micro architecture, and shows how to implement a large instruction window processor without requiring large structures thus permitting a high clock frequency.

It focus on four critical aspects of a micro architecture like scheduling instructions, recovering from branch mispredicts, buffering a large number of stores and forwarding data from stores to any dependent load, and reclaiming physical registers. While scheduling window size is important, it shows the performance of large instruction windows to be more sensitive to the other three design issues.

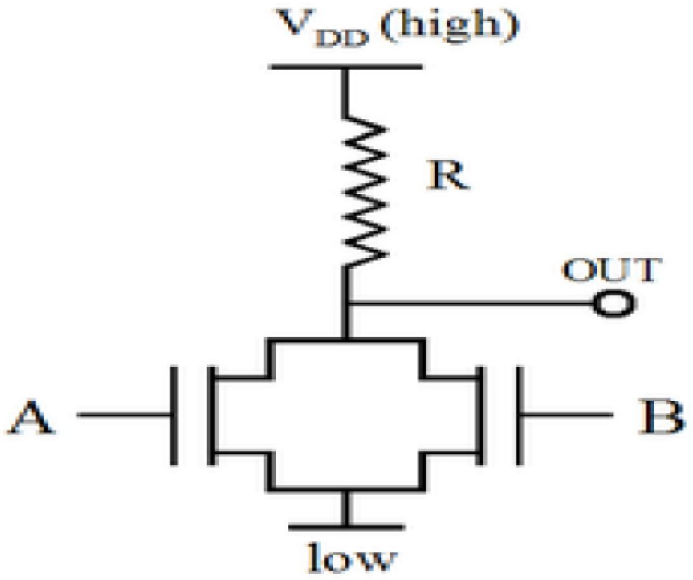

Figure 2. Pull Down Network

2.3 IMPACT OF NBTI AGING ON THE SINGLE-EVENT UPSET OF SRAM CELLS

With CMOS technology scaling, design for reliability has become an important step in the design cycle and increased the need for efficient and accurate aging simulation methods during the design stage. NBTI-induced delay shifts in logic paths are asymmetric in nature, as opposed to the averaging effect due to recovery assumed in traditional aging analysis. Timing violations due to aging, in particular, are very sensitive to the standby operation regime of a digital circuit. By identifying the critical moments in circuit operation and considering the asymmetric aging effects, timing violations under NBTI effect are correctly predicted. A simple analytical model to predict the aging induced delay shifts in a digital gate is presented using device level long-term models. The aging prediction uses the library cell delays without relying on re-characterization of the standard cell library. The proposed reliability analysis is and can be applied to any large scale circuits with minimum overhead time. The concept behind is parametric shifts induced by NBTI do not have a large impact on the single-event upset rate calculations (10%).

2.4 THE NBTI-AWARE PROCESSOR

This paper analyzes the impact of negative bias temperature instability (NBTI) on the single-event upset rate of SRAM cells through experiments and SPICE simulations. The critical charge simulations introducing different degradation patterns in the cells, in three technology nodes, from 180 to 90 nm is performed. The simulations results were checked with -particle and heavy-ion

irradiations on a 130-nm technology. Both simulations and experimental results show that NBTI degradation does not significantly affect the single event upset SRAM cell rate as long as the parametric drift induced by aging is within 10%.Transistors consist of lower number of atoms with every technology generation. Such atoms may be displaced due to the stress caused by high temperature, frequency and current, leading to failures. NBTI degrades PMOS transistors whenever the voltage at the gate is negative (logic input "0"). The main consequence is a reduction in the maximum operating frequency and an increase in the minimum supply voltage of storage structures to cope for the degradation. Many PMOS transistors affected by NBTI can be found in both combinational and storage blocks since they observe a "0" at their gates most of the time. It proposes and evaluates the design of an NBTI-aware processor.

The benefits of the proposed techniques are (i) their practically negligible cost in hardware, (ii) their low delay impact and (iii) the significant NBTI guard-band reduction.

1. The results show guard-band reductions between 12.6% and 18% for the different blocks without impacting any critical path. NBTI degrades PMOs transistor when voltage at gate is negative.
2. Reduction in maximum operating frequency increase in minimum supply voltage.

2.5 NBTI TOLERANT MICROARCHITECTURE DESIGN IN THE PRESENCE OF PROCESS VARIATION

Micro architectural redundancy has been proposed as a means of improving chip lifetime reliability. It is typically used in a reactive way, allowing chips to maintain operability in the presence of failures by detecting and isolating, correcting, and replacing components on a first-come, first-served basis only after they become faulty.

In a recent work in this area, an alternative, more preferred method of exploiting micro architectural redundancy to enhance chip lifetime reliability is proposed. In this approach, redundancy is used proactively to allow non-faulty micro architecture components to be temporarily deactivated, on a rotating basis, to suspend and/or recover from certain wear out effects. This approach improves chip lifetime reliability by warding off the onset of wear out failures as opposed to reacting to them posteriorly. This proactive wear out recovery approach increases lifetime reliability of the cache by about a factor of seven relative to no use of micro architectural redundancy. micro architecture design techniques to combat the combined effect of NBTI and process variation (PV) on the reliability of high-performance Microprocessors.

III. METHODOLOGY AND MATERIALS USED

3.1 COMPLEMENTARY MOS

Complementary Metal–Oxide–Semiconductor is a technology for constructing integrated circuits. CMOS technology is used in microprocessors, microcontroller, static RAM, and other digital circuits. CMOS technology is also used for several analog circuits such as image sensors, data converters, and highly integrated transceivers for many types of communication. CMOS is also sometimes referred to as complementary-symmetry metal–oxide–semiconductor. The words "complementary-symmetry" refer to the fact that the typical digital design style with CMOS uses complementary and symmetrical pairs of p-type and n-type metal oxide semiconductor field effect transistors for logic functions. Advantage of CMOS over NMOS is that both low to high and high to low output transitions are fast since the pull up transistors have low resistance when switched ON unlike the load resistors in NMOS logic. At the same time power dissipation increases.

IV. SRAM TECHNOLOGY

A Static Random Access Memory is designed to fill two needs: to provide a direct interface with the CPU at speeds not attainable by DRAMs and to replace DRAMs in systems that require very low power consumption. In the first role, the SRAM serves as cache memory, interfacing between

DRAMs and the CPU. It shows a typical PC microprocessor memory configuration. SRAM is designed to fill two needs: to provide a direct interface with the CPU at speeds not attainable by DRAMs and to replace DRAMs in systems that require very low power consumption. In the first role, the SRAM serves as cache memory, interfacing between DRAMs and the CPU. It shows a typical PC microprocessor memory configuration.

V. SRAM OPERATION

The SRAM cell consists of a bi-stable flip-flop connected to the internal circuitry by two access transistors .When the cell is not addressed, the two access transistors are closed and the data is kept to a stable state, latched within the flip-flop. The flip-flop needs the power supply to keep the information. The data in an SRAM cell is volatile that the data is lost when the power is removed. However, the data does not "leak away" like in a DRAM, so the SRAM does not require a refresh cycle.

An SRAM cell has three different states. It can be in: standby (the circuit is idle), reading (the data has been requested) and writing (updating the contents). The SRAM to operate in read mode and write mode should have "readability" and "write stability" respectively. The three different states work as follows:

(i) *Standby* -If the word line is not asserted, the access transistors M5 and M6 disconnect the cell from the bit lines. The two cross-coupled inverters formed by M1 – M4 will continue to reinforce each other as long as they are connected to the supply.

(ii) Reading -Assume that the content of the memory is a **1**, stored at Q. The read cycle is started by pre charging both the bit lines to a logical **1**, then asserting the word line WL, enabling both the access transistors.

(iii) Writing -During a read operation these two bit lines are connected to the sense amplifier that recognizes if a logic data —1‖ or —0‖ is stored in the selected elementary cell. This sense amplifier then transfers the logic state to the output buffer which is connected to the output pad.

5.1 MEMORY CELL

Different types of SRAM cells are based on the type of load used in the elementary inverter of the flip-flop cell. There are currently three types of SRAM memory cells.

5.2 4T SRAM CELL

The most common SRAM cell consists of four NMOS transistors plus two poly-load resistors (Figure 3.7). This design is called the 4T cell SRAM. Two NMOS transistors are pass-transistors. These transistors have their gates tied to the word line and connect the cell to the columns. The two other NMOS transistors are the pull-downs of the flip-flop inverters.

The complexity of the 4T cell is to make a resistor load high enough to minimize the current. However, this resistor must not be too high to guarantee good functionality. Despite its size advantage, the 4T cells have several limitations. These include the fact that each cell has current flowing in one resistor the cell is sensitive to noise and soft error because the resistance is so high, and the cell is not as fast as the 6T cell.

5.3 6T SRAM CELL

6T eliminates the above limitations is the use of a CMOS flip-flop. In this case, the load is replaced by a PMOS transistor. This SRAM cell is composed of six transistors, one NMOS transistor and one PMOS transistor for each inverter, plus two NMOS transistors connected to the row line. This configuration is called a 6T Cell.

5.4 NEGATIVE BIAS TEMPERATURE INSTABILITY

Negative bias temperature instability (NBTI) is a considerable reliability concern for sub-micrometer CMOS technologies. NBTI occurs in PMOS devices when the gate source voltage is negative. NBTI increases the threshold voltage, reduces the drive current, which causes degradation in circuit speed and requires a minimum voltage increase in storage cells to keep the content.

5.5 RECOVERY BOOSTING

The basic idea behind recovery boosting is to raise the node voltages of a memory cell in order to put both PMOS devices into the recovery mode. This can be achieved by raising the ground voltage and bit lines to the nominal voltage through an external control signal. Raising the bit lines to Vdd allows for a fast transition into the recovery boost mode, which is important for high-speed SRAM. These can be performed through tanner EDA tool.

VI. CONCLUSION

The fine-grained recovery boosting approach that is evaluated in this paper can be used for small SRAM arrays. The average power consumed during fine grain recovery boosting is reduced and while using coarse grain recovery boosting is lesser. In future work, the use of coarse-grained recovery boosting, which imposes less area overheads, for designing caches can be studied. In this approach, the modified SRAM cell is used instead one of the fine-grained control.

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